# A Mixed-Signal Low-Noise Sigma-Delta Interface IC for Integrated Sub-Micro-Gravity Capacitive SOI Accelerometers

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**A Mixed-Signal Low-Noise Sigma-Delta Interface IC for Integrated Sub-Micro-Gravity Capacitive SOI Accelerometers**

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I dedicate this dissertation to my loving parents for
their supports, encouragements, and wisdom.

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# SUMMARY

Recently, there has been an increasing demand for low-power and small form-factor micro- and sub-micro-gravity MEMS accelerometers for a variety of applications including measurement of the low-frequency content of vibratory disturbances, inertial navigation and geophysical sensing. High-performance accelerometers can also be utilized in ultra-small size for large-volume portable applications such as laptop computers and cellular phones.

This dissertation presents the design and development of a mixed-signal low noise second-order ΣΔ integrated circuit (IC) for the open-loop and closed-loop operation of integrated capacitive micro- & nano-gravity accelerometers. The micromechanical accelerometers are fabricated in thick (>100 μm) silicon-on-insulator (SOI) substrates. The IC provides the 1-bit digital output stream and has the versatility of interfacing sensors with different sensitivities while maintaining minimum power consumption (<5 mW) and maximum dynamic range (>90 dB). A fully-differential sampled-data scheme is deployed with the ability of low-frequency noise reduction through the use of correlated double sampling (CDS) scheme. In this work, the measured resolution of the closed-loop CMOS-SOI accelerometer system, in the presence of high background accelerations, is in the micro-g *(g: gravity)* range. In this design, a second-order SC ΣΔ modulator is cascaded with the accelerometer and the front-end amplifier. The accelerometer operates in air and is designed for non-peaking response with a $BW_{-3dB}$ of 500 Hz. A 22 dB improvement in noise and hence dynamic range is achieved with a sampling clock of 40 kHz corresponding to a low oversampling ratio *(OSR)* of 40. The interface IC consumed a current of 1.5 mA from a supply of 3 V.

# CHAPTER 1

# INTRODUCTION

## 1.1 OVERVIEW

Microelectromechanical systems (MEMS) are small integrated devices that are usually fabricated on a silicon substrate and combine electrical and mechanical elements for sensing or actuating purposes. While the support electronics are implemented using IC fabrication processes, micromechanical components are fabricated through micromachining sequences that selectively remove parts of the silicon or add new structural layers to form the three-dimensional electromechanical elements. Examples of MEMS components include micromirrors, RF MEMS switches, microresonators, microaccelerometers, and microgyroscopes [1–5]. Other new applications are rising as existing technologies are applied to miniaturize and integrate conventional devices.

Micromachined accelerometers are one of the most important classes of MEMS devices that hold the second largest sales capacity after the pressure sensors. There are a wide range of applications that require acceleration measurement such as automotive safety and stability, biomedical applications, oil and gas exploration, and computer accessories. Moreover, high-resolution and high-accuracy accelerometers [57] are required in specific areas including earthquake detection, GPS-augmented inertial navigation, spacecraft guidance/stabilization, and geophysical sensing. High-performance accelerometers can also be utilized in ultra-small size for large-volume portable applications such as laptop computers and cellular phones.

Non-resonant capacitive displacement sensing is a common transduction mechanism exploited in microaccelerometers, which provides high sensitivity and resolution, low temperature dependency, good DC response, and good noise performance compared to other mechanisms of the acceleration measurement such as resonance, tunneling, piezoresitive, and piezoelectric [6–9]. Capacitive microaccelerometers reduce footprint, cost and weight and commence new market potentials for consumer applications with better performance and redundancy. Currently, high-performance mixed-signal interface circuits have received growing attention towards higher-level of integration, power reduction and noise cancellation (improved resolution). The new generation of microaccelerometer interface architectures should have the versatility of interfacing with sensors of various sensitivities while maintaining low power consumption, small drift, increased functionality, and large dynamic range [10–14].

There are two main categories of capacitive interface architectures: continuous-time and discrete-time. Continuous-time circuits include resistors, capacitors and op amps. They are more suitable for discrete-component designs because absolute tolerances of integrated resistors and capacitors are not good enough to monolithically achieve high-linearity and high-accuracy analog signal conditioning [15]. Also, the requirement for large resistors and capacitors is another limitation that makes it difficult to implement these architectures in an integrated format. Therefore, analog sampled-data techniques have been utilized to replace resistors resulting in switched-capacitor (SC) circuits that consist of MOSFET switches, capacitors and op amps. Different sampled-data interface ICs for microaccelerometers have been previously reported in literature [16–21]. One important reason for the success of SC circuits is that the accuracy of the signal processing system is proportional to the relative accuracy of capacitors. Primary features of SC circuits include CMOS compatibility,

good accuracy of time constants, good voltage linearity, and good temperature characteristics [15]. They also improve low-frequency noise through correlated double sampling (CDS) or chopper stabilization techniques and can provide a direct digital output [22–25]. Their primary disadvantages are clock feedthrough, charge injection, requirement for non-overlapping clocks, and input bandwidth limitation.

## 1.2 HISTORY

Due to the low-cost and high-volume demand, the majority of commercially available MEMS accelerometers have been automotive grade i.e., milli-g resolution in a few-g dynamic rage. Analog Devices, Inc (ADI) is one of the most successful pioneers in developing inertial microsystems [26]. The ADXL50 was the first integrated microaccelerometer commercialized by ADI for automotive applications that was fabricated through a 2 μm thick polysilicon surface micromachining process in 1991 [26]. The ADXL40 [26] is a new generation of microaccelerometers that is fabricated on 10 μm thick silicon-on-insulator (SOI) wafers with higher resolution (sub-milli-g range) and smaller size (Figure 1.1). ADI had shipped over one hundred million accelerometers by the end of year 2002 and since then has maintained its leadership position as the industry's largest volume supplier of single-chip MEMS accelerometers and integrated MEMS gyroscopes. The ADXRS150/300 is the only commercially available device that integrates both an angular rate sensor and signal processing electronics onto a single piece of silicon [27]. Figure 1.2 shows the functional block diagram of the ADXL250, a fully integrated dual axis capacitive microaccelerometer from ADI with signal conditioning on a monolithic IC [28].

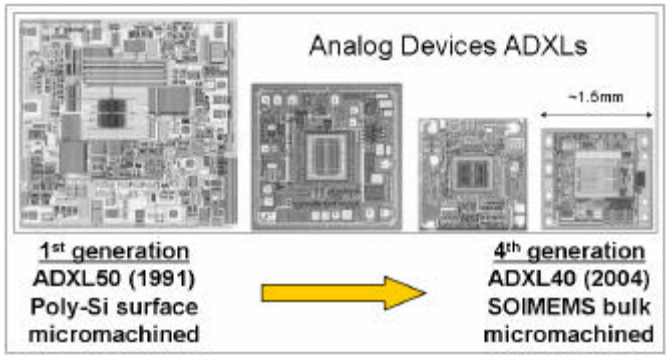



Figure1.1: The microaccelerometer family of ADI [26].

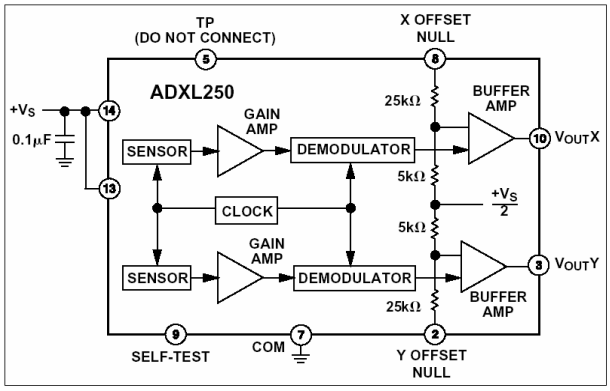



Figure 1.2: Functional block diagram of ADXL250 [28].

This accelerometer operates in an open-loop configuration, suggesting that sufficient linearity and accuracy is achievable without force-feedback scheme. It has a resolution of 1 mg/√Hz with a dynamic range (DR) of 80 dB.

During the past few years, there has been an increasing demand for low-power and small form-factor micro- and sub-micro-gravity MEMS accelerometers. Sub-micro-gravity accelerometers are required for measurement of vibration on platforms installed on earth, space shuttles, and space stations as well as gravity gradiometry and earthquake detection. Conventional systems are bulky, complex and expensive, and consume a lot of power [29]. For example, Figure 1.3 shows an integrated triaxial accelerometer designed to measure general environmental vibrations from ZIN Technologies [30]. It measures 3.5 inches in height by 3.6 inches in width by 4.4 inches in length and consumes a power of 1.65 W (from a supply of 30 V).


Figure 1.3: A triaxial micro-gravity accelerometer from ZIN Technologies [30].

In response to such performance needs, high sensitivity capacitive MEMS accelerometers have been introduced using a variety of surface [31–38] and bulk micromachining [39–46] techniques. In surface micromachined devices, the thickness of the deposited layer and hence, the proof mass is small, causing limitations on the performance of accelerometers. Typically, the resolution of commercial surface-micromachined accelerometers is in the milli-g range. On the other hand, bulk micromachining provides larger proof mass and larger capacitive area that leads to a higher resolution and greater sensitivity.

Researchers at the Carnegie Mellon University have introduced a unique approach to the MEMS capacitive accelerometers [19]. They have developed a new post-CMOS micromachining technology that enables the integration of micromechanical structures with conventional CMOS circuits [20] [35] [37]. In this method, the microstructure and the lateral sense capacitance are fabricated through electrically isolated, multi-metal routings with an overall-thickness of 5 μm. The isolating composite structure is integrated with the electronics to increase transducer sensitivity by minimizing parasitic capacitances. In this process, fabricated microaccelerometers are very tiny (350 μm × 500 μm) with a very small proof mass (<1 micro-gram) causing the mechanical noise to increase and the electrical sensitivity to decrease. The best reported resolution is 50 μg/√Hz at 400 Hz in a linear range of ±7g [38].

Researchers at the University of Michigan demonstrated a bulk-micromachined accelerometer system with micro-gravity resolution in their recent publications [41–46]. However, their fabrication process is complex and requires a number of steps, combining surface and bulk micromachining. Moreover, high temperature steps make the fabrication technology not CMOS-compatible [41]. In addition, the large capacitive area along with the small stiffness of those devices makes them susceptible to stiction during the wet-release process, which reduces yield. The used interface circuit is generally a closed-loop electromechanical ΣΔ modulator, including the sensor's transfer function in the forward loop (Figure 1.4). Five different clock phases are required for the proper operation of the system (see Figure 1.4). The chopper stabilization scheme is used for the low-frequency noise suppression [45]. However, there has been no clear explanation on how effectively the low-frequency noise is suppressed using copper stabilization.

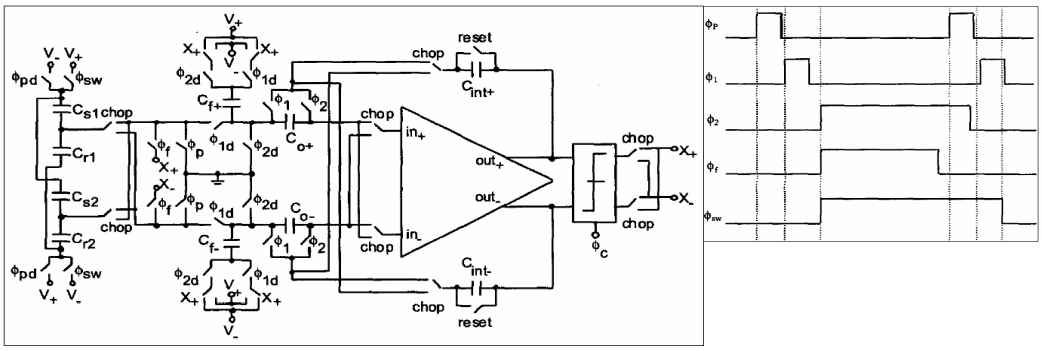



Figure 1.4: Schematic view of a fully-differential front-end interface circuit [45].

Our group has been working on a project (funded by NASA) to fundamentally explore accuracy and resolution limits of capacitive microaccelerometers with a goal of achieving sub-micro-gravity resolution and stability (<200 nano-g) in an integrated cost-effective implementation. There has been no investigation of sub-micro-gravity MEMS accelerometers in the past.

## 1.3 MOTIVATION

Bulk-micromachined accelerometers will dominate the next generation of high-resolution, high-accuracy microaccelerometers. They are utilized in more products, particularly as the technology continues to drive the development of brand new products. Their fabrication processes become simpler and provide electronics integration. Their large proof mass and high sensitivity push the resolution down to sub-micro-g level and the electronic noise floor is no longer a limiting factor. However, their transduction capacitances are large (in the range of 10's of pF), which put limitations on current interface circuit architectures in terms of die size, power dissipation and speed. Therefore, new interface circuits are required to provide more functionality without compromising the area, power and speed.

The objective of this dissertation is to design and implement a sampled-data front-end followed by an optimized-performance second-order ΣΔ modulator to readout and control a new micro-g bulk-micromachined SOI accelerometer. The performance of the interface IC is not limited by the large value of the sense capacitance and provides micro- & sub-micro-g overall resolution. The accelerometer's capacitive sensitivity (*DC/gravity*) is increased by reducing the gaps through post-deposition of doped low pressure chemical vapor deposited (LPCVD) polysilicon. The mechanical noise floor per unit area is improved by keeping thick silicon seismic mass on the backside of the sensor. In contrast to the previously reported ΣΔ microaccelerometers, in which the mechanical transfer function of the sensor was typically the only element of the loop-filter [43], in our design, a switched-capacitor (SC) second-order ΣΔ modulator is cascaded with the accelerometer and the front-end amplifier. High capacitive sensitivity eliminates high gain requirement of the front-end and helps with better

quantization noise shaping [89]. The accelerometer operates in air and is designed for non-peaking response with a $BW_{-3dB}$ of 500 Hz. By including the low-pass transfer function of the sensor in the forward loop, the closed-loop system helps with better reshaping of the inter-stage circuit noises. Since the mechanical bandwidth of sub-micro-g SOI accelerometers can not be very small in a microscaled accelerometer, the overall noise bandwidth can be further reduced by the electronics (<10 Hz). The accelerometer is wirebonded to the interface circuit. However, there is a potential to integrate the MEMS device with the IC chip on the same SOI substrate if IC fabrication on the thick SOI wafer is accessible. To improve the noise performance of sub-micro-gravity (<200 ng) capacitive accelerometers, the proof mass should be very large (10-30 milli-gram) and the capacitive sensitivity should be also large (20-50 pF/g) [47]. Investigation of the circuit and sensor requirements to achieve deep sub-gravity resolution and stability is the other major task.

This dissertation is organized in seven chapters. **CHAPTER 1** briefly introduces the history of the MEMS accelerometers and the motivation behind our work. **CHAPTER 2** discusses the accelerometer's principle of operation and determines the technological requirements for improving the resolution and stability of the sensor. The electromechanical design equations of the in-plane capacitive microaccelerometer are introduced. Two novel accelerometer's fabrication processes are developed that enable the implementation of high yield and high performance capacitive SOI accelerometers with micro- and sub-micro-g resolution and stability. The design specifications of high aspect ratio dry-released SOI accelerometers are provided and two fabricated micro- and sub-micro-g SOI accelerometers are presented. **CHAPTER 3** introduces a new input switching scheme for a front-end SC charge amplifier with analog output that eliminates area-consuming on-chip reference capacitors. Open-loop

static and dynamic characteristics of the micro-g SOI accelerometer wirebonded to the CMOS IC are obtained. **CHAPTER 4** presents a low-power high-performance SC interface circuit to readout the sub-micro-g SOI accelerometer. The very low-bandwidth requirement of the sub-micro-g CMOS-SOI accelerometer system necessitates significant low-frequency noise reduction and band limiting that are addressed in details. Sub-micro-g performance results of the accelerometer wirebonded to the chip are provided. **CHAPTER 5** introduces the development of an open-loop ΣΔ CMOS-SOI accelerometer system with an acceleration resolution of 110 μg/√Hz and a dynamic range of 85 dB. This architecture relies on a front-end charge amplifier and a back-end first-order SC ΣΔ modulator with an output bitstream. It is explained in details how the back-end ΣΔ modulator is effectively decoupled from the sensor (to achieve optimized performance regardless of the sensor capacitance). A complete static and dynamic characteristic of the entire system is reported. **CHAPTER 6** discusses the implementation and characterization of a force-rebalanced high-order ΣΔ CMOS-SOI accelerometer with micro-gravity resolution and stability and an extended dynamic range of 95 dB. System-level modeling and simulation of the entire closed-loop accelerometer are performed that are used as design and analysis guidelines for the circuit-level implementation. Simulation results are evaluated through the silicon-implementation of the closed-loop ΣΔ CMOS-SOI accelerometer and measurement results are obtained. **CHAPTER 7** briefly summarizes the research contributions and gives recommendations to impalement biaxial and triaxial SOI accelerometers and interface circuits as the future directions.

# CHAPTER 2

# SOLID MASS CAPACITIVE SOI ACCELEROMETERS

## 2.1 OVERVIEW

A silicon-on-insulator (SOI) wafer is a layered structure consisting of a silicon layer (50 nm-150 μm) on top of an insulating substrate (usually silicon dioxide) and another thick silicon layer. Thick SOI wafers have become the substrate of choice for many high-performance MEMS devices such as microgyroscopes and multi-axis optical micromirrors [48] [49]. The use of thick SOI substrates in implementing lateral capacitive accelerometers has the advantage of increased mass compared to the polysilicon surface micromachined devices [50–52], which results in reduced Brownian noise floor. The performance of bulk silicon accelerometers is typically limited by the electronic noise floor, which can be improved with increasing the sensitivity (*DC/gravity*) of the accelerometer [53–55]. To achieve higher sensitivities, one should increase the capacitive area, reduce the capacitive gap size, and reduce the mechanical stiffness of the device, which in turn increases the possibility of stiction in the release step. [56–58]. Therefore, processing techniques that avoid wet release of the microaccelerometer while maintaining high sensitivity per unit area are of interest. Figure 2.1 shows the schematic diagram of an *in-plane* capacitive SOI accelerometer with a solid seismic mass. A solid proof mass with no perforation results in more than 25% increase in mass per unit area, smaller form-factor and improved mechanical noise performance.

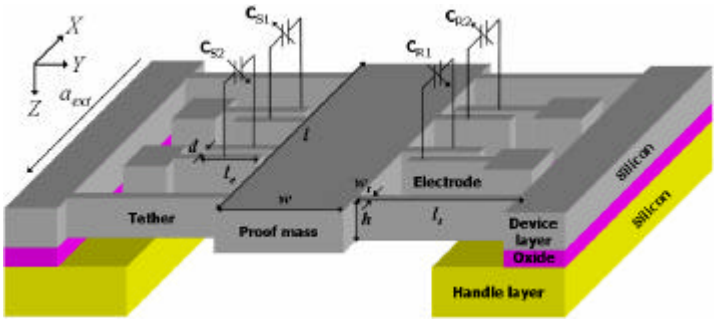



Figure 2.1: Schematic diagram of a lateral capacitive SOI accelerometer.

The proposed SOI accelerometers are fabricated through a backside dry-release process that eliminates the need for release holes in the proof mass. It is also possible to keep some part of the silicon handle layer in the back of the proof mass to add more mass and improve the performance (Figure 2.2).

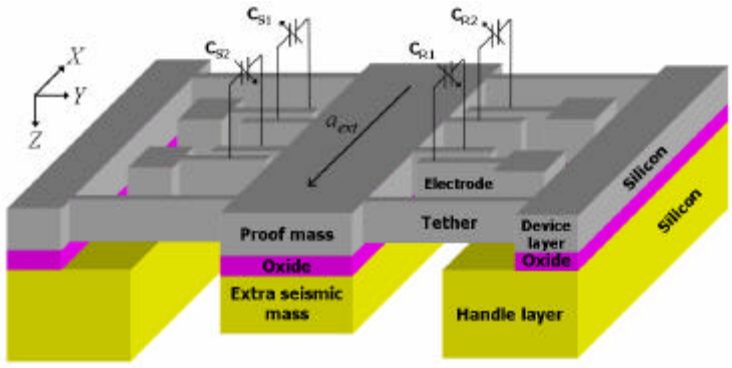



Figure 2.2: Schematic diagram of an SOI accelerometer with added seismic mass.

In this chapter, the design and implementation of high-resolution and high-accuracy capacitive SOI accelerometers in low-resistivity (< 0.01 Ω.cm) thick SOI substrates are presented. It will be explained how the resolution and sensitivity of the dry-released SOI accelerometers are each improved by 10× to achieve, for the first time, deep sub-micro-gravity resolution in a small footprint (<0.5 $cm^2$).

## 2.2 PRINCIPLE OF OPERATION

The simplified lumped-element model of a differential capacitive microaccelerometer is shown in Figure 2.3.

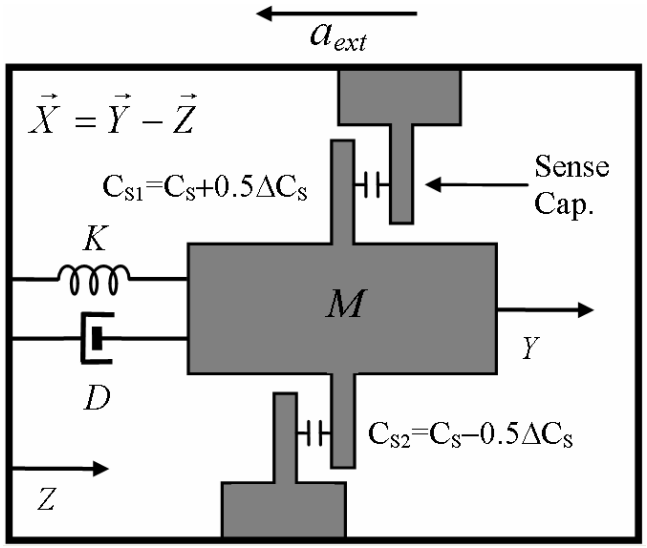



Figure 2.3: Lumped-element model of a capacitive microaccelerometer.

The accelerometer consists of a seismic proof mass *(M)* that responds to the external acceleration *($a_{ext}$)* with respect to its frame *(X=Y-Z)* in line with the sense direction. Four tethers *(K)* suspend the proof mass, and the surrounding air imposes the squeeze film damping *(D)* on the structure. The movement of the proof mass causes the inter-electrode capacitors to change, and the interface circuit detects minute changes of the sensor's capacitance. Dynamic behavior of the sensor is governed by the Newton's second law of motion:

$$M\frac{d^2x}{dt^2} + D\frac{dx}{dt} + Kx = F_{ext} = -Ma_{ext} \tag{2-1}$$

The effective spring constant *(K)* of the accelerometer is expressed by [59]

$$K = K_{mechanical} - K_{electrical} \quad [N/m] \tag{2-2}$$

The mechanical and electrical stiffness of the structure are given by [60]

$$K_{mechanical} = 4E_x h\left(\frac{w_t}{l_t}\right)^3 \tag{2-3}$$

$$K_{electrical} = \frac{1}{2}V_{DC}{}^2 \frac{N_e e_0 h l_e}{d^2} \tag{2-4}$$

where $E_x$ is the Young's modulus of silicon in the sense direction; $h$, $w_t$ and $l_t$ are the height, width and length of the tethers, respectively; $N_e$ is the total number of sense electrodes with the length of $l_e$ and initial gap spacing of $d$; $V_{DC}$ is the applied DC voltage to the sense capacitors. Accelerometers are designed such that $K_{electrical} << K_{mechanical}$. The air pressure distribution in the gap is modeled by the Reynolds equations [61] [62]. By integrating the pressure over the surface of the electrodes, one can obtain the force imposed by the air flow [63] [64]. The damping coefficient *(D)* is then calculated through dividing the force by the proof mass velocity. In [65] and [95], an analytical formula for the air squeeze film damping is introduced which is valid for bulk microaccelerometers with micrometer gaps:

$$D = N_e h_{eff} l_e \left(\frac{h}{d}\right)^3 \tag{2-5}$$

$h_{eff}$ is the effective viscosity of air ($18.5\times10^{-6}$ Ns/m$^2$). It is assumed that the length of the electrodes *($l_e$)* is larger than the height of the electrodes *(h).* The fundamental sense limit is set by the Brownian noise equivalent acceleration *(BNEA)* of the suspended mass. This acceleration (caused by air molecules' collisions) is expressed as [66] [67]

$$BNEA = \frac{\sqrt{4k_B TD}}{M} = \sqrt{\frac{4k_B T w_0}{MQ}} \propto \sqrt{\frac{h}{(capacitive\ gap)^3}} \qquad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{2-6}$$

In this equation, $k_B$ is the Boltzmann constant; $T$ is the absolute temperature; $w_0 = \sqrt{K/M}$ is the accelerometer natural angular frequency (first flexural mode); $Q = Mw_0/D$ is the mechanical quality factor. Increasing the mass and reducing the air damping improves the mechanical noise floor. However, reducing the damping increases the possibility of resonant behavior (high-$Q$) and sensitivity to higher order mechanical mode shapes that are not desirable. Another limiting factor is the circuit noise equivalent acceleration *(CNEA)* that depends on the capacitive resolution of the interface circuit *($DC_{MIN}$)* and the capacitive sensitivity ($S$) of the accelerometer *(S=DC/gravity)*:

$$CNEA = \frac{\Delta C_{MIN}}{S} \qquad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{2-7}$$

The static sensitivity of a differential accelerometer *(S)* is equal to [65]

$$S = \frac{N_e e_0 h l_e}{d^2}\frac{M}{K} = \frac{2C_S}{d}\frac{1}{w_0^{\,2}} \propto \frac{h}{\left(capacitive\ gap\right)^2} \qquad \left[\frac{F}{m/s^2}\right] \tag{2-8}$$

In this equation, $C_S$ is half of the rest (initial) capacitance in between the proof mass fingers and the sense electrodes. Finally, the total noise equivalent acceleration *(TNEA)* of the accelerometer is expressed as

$$TNEA = \sqrt{BNEA^2 + CNEA^2} \qquad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{2-9}$$

The design objective is to minimize the *BNEA* and *CNEA* per unit area.

## 2.3 DESIGN AND FABRICATION OF CAPACITIVE MICRO-GRAVITY SOI ACCELEROMETER

Micro-gravity accelerometers are fabricated in 50 μm thick SOI wafers using a high yield, backside dry-release, low-temperature process comprising of two masks and only three plasma-etching steps. In this implementation, capacitive gaps are created using deep reactive ion etching (DRIE) (also known as the Bosch process) [68]. High sensitivity and low mechanical noise floor per unit area, which are important requirements to achieve micro-gravity resolution, are provided through a thick solid proof mass with no perforation. The use of a solid proof mass increases the mass per unit area by more than 25%, which results in further reduction of the *BNEA* and further increase of the sensitivity (Equations (2-6) and (2-8)).

### 2.3.1 ELECTROMECHANICAL DESIGN

In this design, the overall accelerometer's area was 5 mm × 6 mm. The sense electrodes' pitch was selected to 60 μm to make the fingers stiff enough to avoid nonlinearities caused by the fingers' vibration and to place 90 sense electrodes along the length of the proof mass. The length of electrodes was selected to 500 μm. Since the reliably achievable gap aspect ratio *(AR=h/d)* in DRIE is typically limited to 20:1 to 30:1, increasing the thickness of the device layer improves the *BNEA* but it deteriorates the sensitivity of the device (Equation (2-8)). In other words, for a constant aspect ratio, increasing the thickness of the device layer increases the capacitive gap *(d)*, which in turn improves the *BNEA* (Figure 2.4), but reduces the sensitivity (Figure 2.5), which consequently degrades the *CNEA* (Figure 2.6). In order to improve the sensitivity, the number of sense fingers must be increased and the

effective stiffness must be reduced that causes the device to be severely vulnerable to the stiction during the release step and normal operation. Therefore, avoiding wet etching steps in the fabrication process is crucial. The *TNEA* is rephrased as

$$TNEA^2 = BNEA^2 + CNEA^2 = k_{BNEA}\frac{h}{d^3} + k_{CNEA}\frac{d^4}{h^2} = k_{BNEA}\frac{(AR)}{d^2} + k_{CNEA}\frac{d^2}{(AR)^2} \quad (2\text{-}10)$$

$$k_{BNEA} = \frac{4k_B T N_e h_{eff} l_e}{r_{si}^2 A_P^2} \quad \left[ m^4 / s^4 \sqrt{Hz} \right] \quad (2\text{-}11)$$

$$k_{CNEA} = \frac{w_0^4 \Delta C_{MIN}^2}{N_e^2 e_0^2 l_e^2} \quad \left[ 1 / s^4 \sqrt{Hz} \right] \quad (2\text{-}12)$$

where $A_P$ is the top area of the solid proof mass, *AR* is the DRIE trench aspect ratio, and $r_{si}$ is the volume density of silicon. The design objective is to minimize the *TNEA* through minimizing the *BNEA* and maximizing the static sensitivity *(S)* while satisfying process simplicity and size limitations. Since the sense gap size is limited by the *AR*, one can find an optimum gap size to minimize the *TNEA* by evaluating the derivative of Equation (2-10) with respect to *d* at zero (Figure 2.7).

$$d_{OPT} = \sqrt[4]{\frac{k_{BNEA}}{k_{CNEA}}(AR)^3} \quad (2\text{-}13)$$

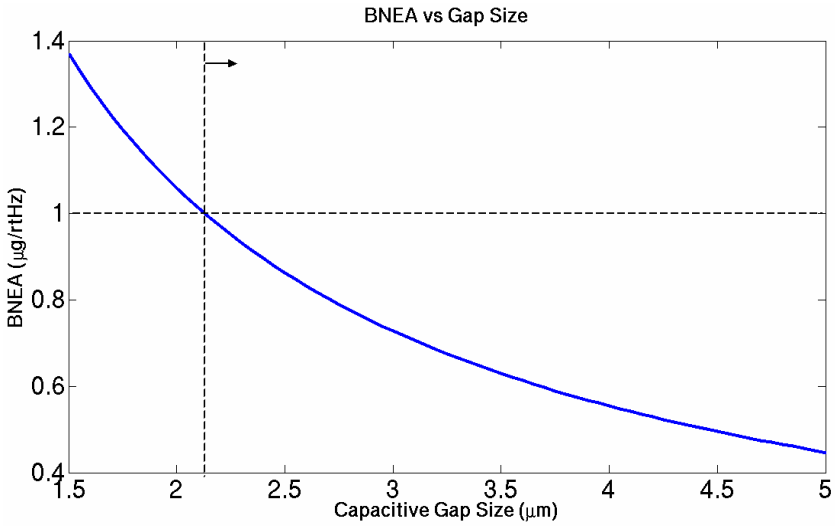



Figure 2.4: *BNEA* vs. capacitive gap changes.

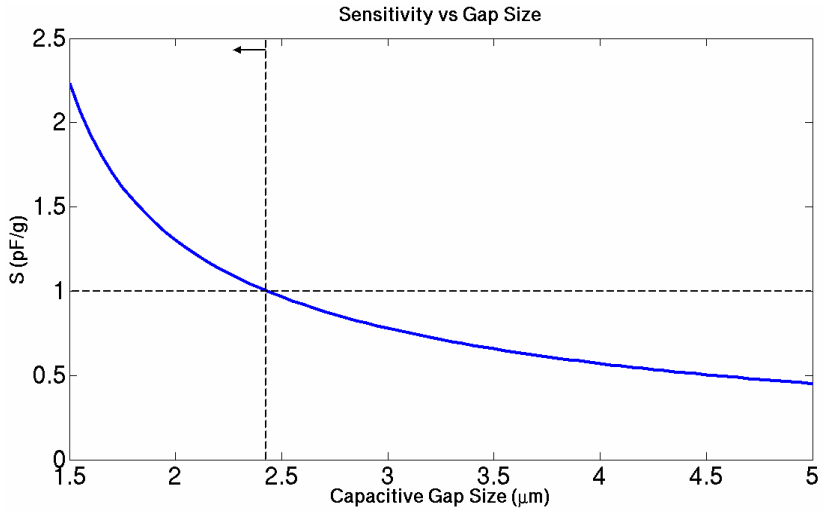



Figure 2.5: Static sensitivity vs. capacitive gap changes.

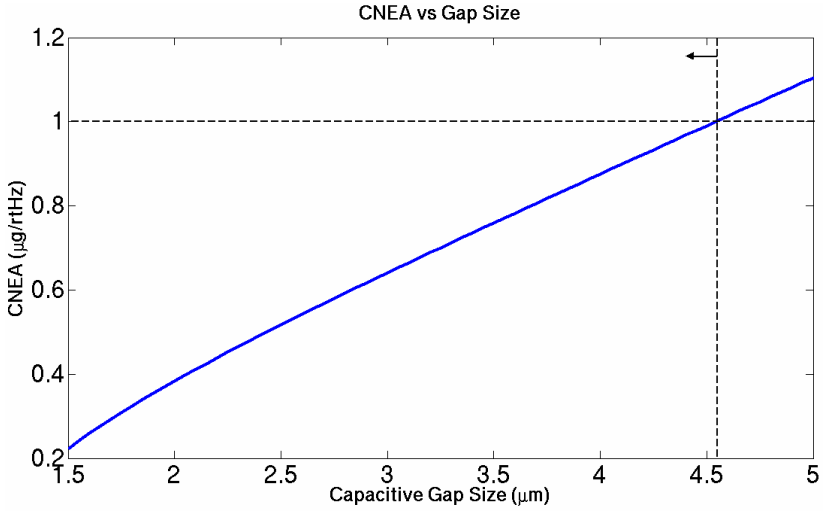



Figure 2.6: *CNEA* vs. capacitive gap changes.

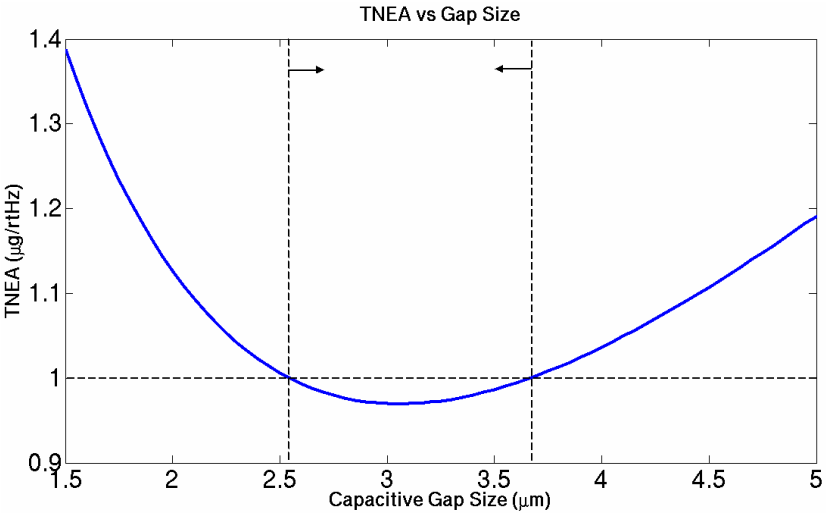



Figure 2.7: *TNEA* vs. capacitive gap changes.

Therefore, an optimum SOI thickness is obtained to maximize the sensitivity and minimize the mechanical noise floor.

$$h_{OPT} = (AR) \times d_{OPT} = (AR) \times \sqrt[4]{\frac{k_{BNEA}}{k_{CNEA}} (AR)^3} \qquad (2\text{-}14)$$

For this implementation and considering an *AR* of 20:1, the optimized SOI thickness is about 50 µm with an optimized gap size of 2.5 µm. The optimized *TNEA* is 1 µg/√Hz. To avoid mechanical oscillation and achieve non-peaking transfer function (for additional noise filtering through the sensor), the damping factor should be large, which is detrimental to the *BNEA*. Therefore, in the design process, variation of *Q* versus gap size should be monitored (Figure 2.8).

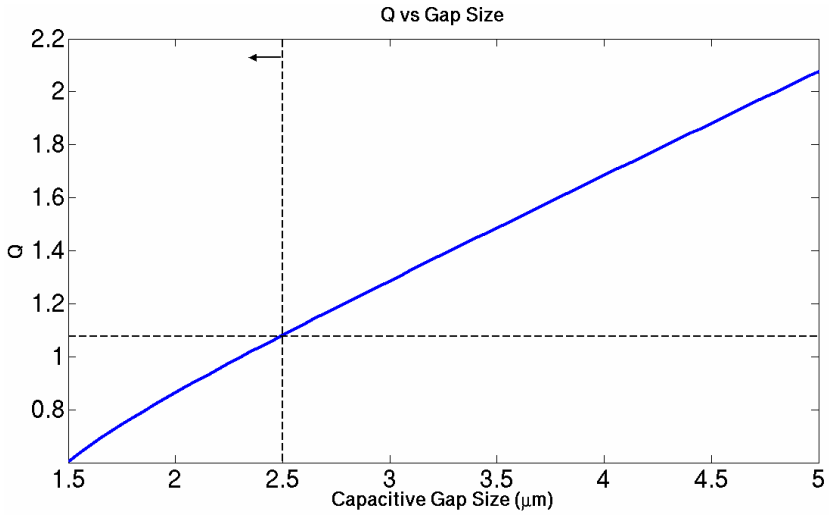



Figure 2.8: Quality factor vs. capacitive gap changes.

A capacitive gap size in the range of 2 to 3 µm satisfies the required performance. Table 2.1 provides the target specifications of a micro-gravity SOI accelerometer.

Table 2.1: Target specifications of a micro-gravity SOI accelerometer.

| | |
|---|---|
| Proof mass size | 2 mm × 6 mm |
| Overall sensor size | 5 mm × 6 mm |
| Device thickness | 50 µm |
| Capacitive gap size | 2.5 µm |
| Static sensitivity | 0.8 pF/g |
| Brownian noise floor | 0.8 µg/√Hz |
| *CNEA* | 0.5 µg/√Hz for $\Delta C_{MIN}$=0.5 aF/√Hz |
| *TNEA* | 1 µg/√Hz |
| Number of sense electrodes | 180 |
| Length of sense electrodes | 500 µm |
| 1$^{st}$ flexural mode | 2 kHz |
| *Q* | 1.1 |

An ANSYS® modal analysis was used to verify the mechanical behavior of the structure. The first flexural mode (in-plane motion) happens at 1.6 kHz (Figure 2.9). The second and the third modes are the out-of-plane and torsional motions that are apart from the in-plane mode. The accelerometer operates in air to avoid resonance (low-*Q* operation).

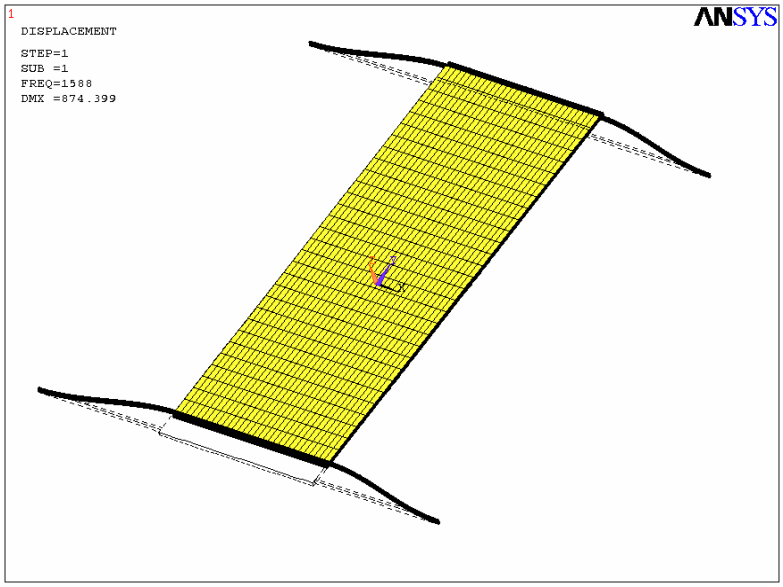



Figure 2.9: ANSYS® modal analysis of the designed microaccelerometer.

Figure 2.10 shows the measured frequency response of the accelerometer in low-level vacuum that agrees with the ANSYS prediction.

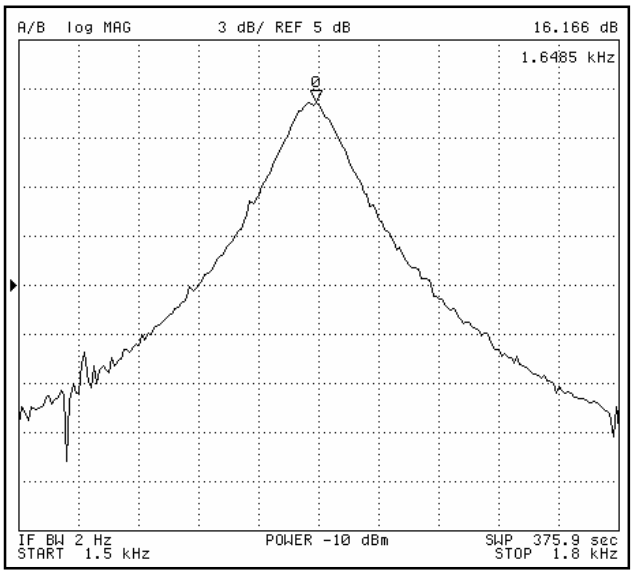



Figure 2.10: In-plane frequency response of the fabricated accelerometer.

### 2.3.2 FABRICATION PROCESS

Fabrication process flow of the SOI accelerometer is shown in Figure 2.11.

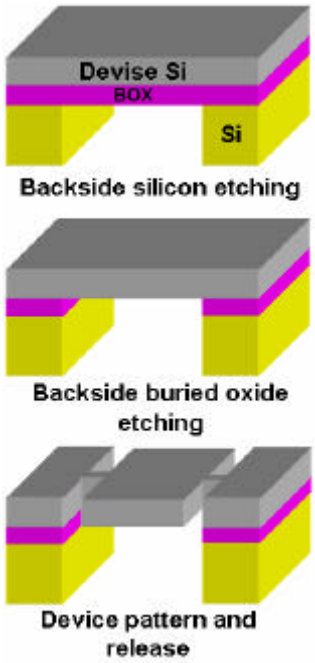



Figure 2.11: Fabrication process flow of a micro-gravity SOI accelerometer.

We start with a low-resistivity *(r=0.01 W.cm)* thick SOI wafer. The silicon under the proof mass is first removed from the backside of the wafer by etching the handle silicon layer all the way to the buried oxide (BOX). This silicon etching is fulfilled in an inductively coupled plasma (ICP) system using the Bosch process. The BOX is then dry-etched in a reactive ion etching (RIE) system. The wafer is flipped and the top layer is patterned all the way through the thickness of the device layer, forming the proof mass with capacitive gaps of 2.3 μm. Since the accelerometers are released from the backside, no release holes in the proof mass are required. Figure 2.12 shows the scanning electron microscopy (SEM) pictures of the final accelerometer.

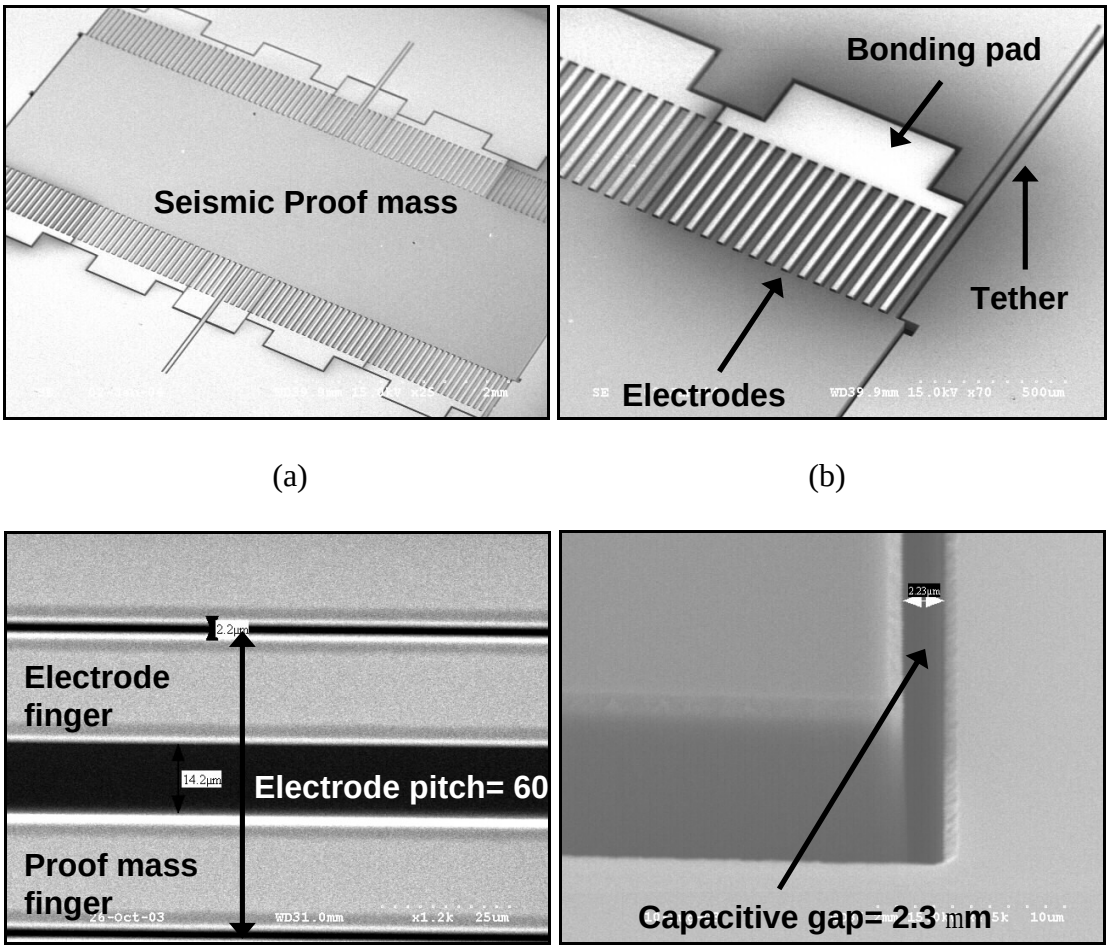



Figure 2.12: SEM of a fabricated device; (a) Top view; (b) Close-up view of the tether and sense electrodes; (c) Electrode pitch; (d) Close-up view of the capacitive gap.

The bonding pad area is minimized to reduce the parasitic pad capacitance. The buried oxide of the SOI substrate provides electrical isolation between the electrodes. If a CMOS process is carried out on an SOI wafer, then the MEMS device can be fabricated on the same substrate after CMOS processing is completed (CMOS post-processing). Bonding pads, which are electrically isolated from each other and the IC, are then wirebonded to the CMOS chip (Figure 2.13). The metalization on the accelerometer bonding pads are performed simultaneously during CMOS metallization and hence no extra mask is needed for this step.

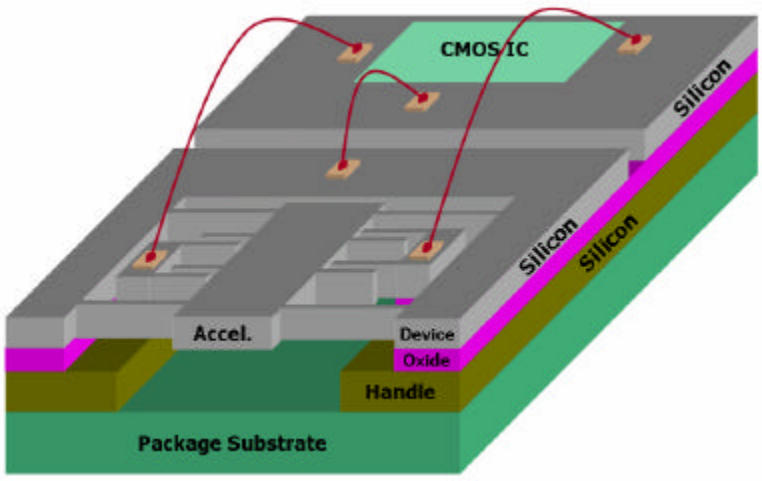
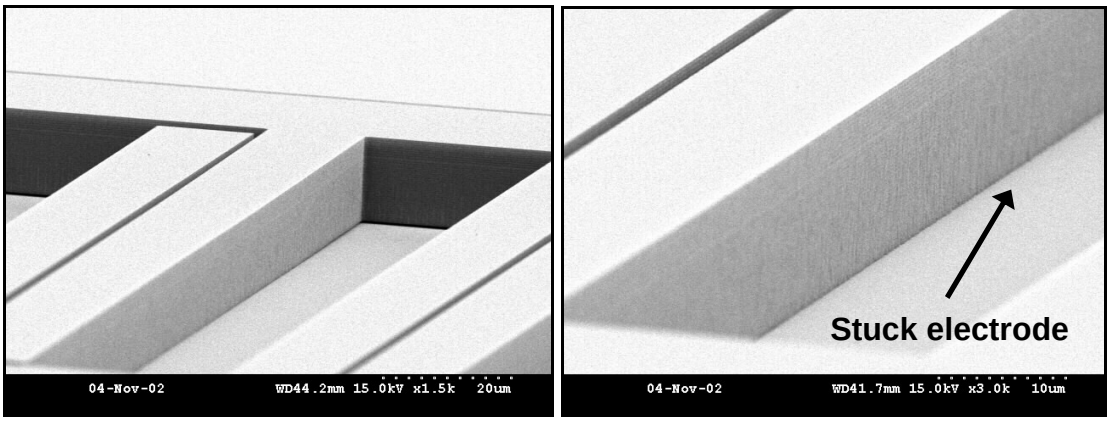



Figure 2.13: MEMS-CMOS on the thick SOI wafer (single-chip solution).

Although the current devices are made in low-resistivity SOI, the use of CMOS-grade wafers will not result in degradation in the performance since the resistance of series CMOS switches is in the range of 1-10 kΩ, which is much greater than the CMOS wafer resistance. The low-temperature processing is another important factor that helps in the CMOS compatibility of this implementation.

It should be mentioned that our previous attempt to release high sensitivity SOI accelerometers with very compliant perforated proof mass from the front-side (using liquid HF through release holes) resulted in severe stiction between the proof mass and the handle silicon layer. Figure 2.14 illustrates stiction in a front-side wet-

released device, which can not be avoided even by critical point drying after the wet release. In contrast, the backside dry-released devices do not suffer from stiction at all and have solid proof mass with no perforations.




(a) (b)

Figure 2.14: (a) SEM showing stiction in devices with no backside etching; (b) Close-up view of a stuck electrode.

The following is a list of unique features of this implementation:

- Very simple (2 masks) high-yield process → Reduced manufacturing cost
- Fully dry-release → Stictionless
- Very compliant mechanical structure → High sensitivity and low *CNEA*
- No perforation in the proof mass → Large solid proof mass and low *BNEA*
- Larger proof mass per unit area → Small form-factor
- Micro-gravity mechanical noise floor → Wide applications
- Low temperature and CMOS compatible → Integrated Single- or two-chip solution

Design specifications of the micro-gravity SOI accelerometer are summarized in Table 2.2.

Table 2.2: Design specifications of the micro-gravity SOI accelerometer.

| | |
|---|---|
| Proof mass size | 2 mm × 6 mm |
| Overall sensor size | 5 mm × 6 mm |
| Device thickness | 50 μm |
| Capacitive gap size | 2.3 μm |
| Aspect ratio *(AR)* | 50:2.3 |
| Mass *(M)* | 1.6 milli-gram |
| Effective Stiffness *(K)* | 100 N/m |
| Air squeeze-film damping *(D)* | 0.013 Ns/m |
| Quality factor *(Q)* | 0.9 |
| Rest capacitance *($C_S$)* | 7.5 pF |
| Static sensitivity | 1 pF/g |
| *BNEA* | 1 μg/√Hz |
| Sensor bandwidth | 1.5 kHz |
| Pull-in voltage | 4.5 V |

## 2.4 DESIGN AND FABRICATION OF CAPACITIVE SUB-MICRO-GRAVITY SOI ACCELEROMETER

In the previous section, capacitive SOI accelerometers with micro-gravity resolution and sensitivity (in the order of 1 pF/g) have been introduced. In this section through innovation in process, the resolution and sensitivity of the dry-released SOI accelerometers are each improved by 10× to achieve sub-micro-gravity resolution within a small size (<0.5 $cm^2$). The figure-of-merit, defined as the ratio of the device sensitivity to its mechanical noise floor, is improved by increasing the solid seismic mass with saving some part of the handle layer attached to the proof mass (as shown in Figure 2.2). Also, capacitive gap sizes are reduced by deposition of doped low pressure chemical vapor deposited (LPCVD) polysilicon, which relaxes the trench etching process and allows for higher trench aspect ratios (>30:1) in thick SOI wafers. The very low bandwidth requirement (<10 Hz) of sub-micro-gravity accelerometers necessitates significant low-frequency noise reduction and band limiting, which are achieved through electronics.

### 2.4.1 ELECTROMECHANICAL DESIGN

The sensor's target specifications are listed in Table 2.3. Goal objectives are achieved for the open loop operation in air. The shock resistivity is a very important characteristic of the accelerometer that should be considered in the design process. As explained in Equation (2-6), increasing the mass and reducing the damping improves *BNEA***.** However, reducing the damping increases the sensitivity to other mode shapes, which is not desirable.

Table 2.3: Target specifications of a sub-micro-gravity SOI accelerometer.

| | |
|---|---|
| Proof mass size | 5 mm × 7 mm |
| Overall sensor size | 7 mm × 7 mm |
| Device thickness | 100 μm |
| Initial capacitive gap | 9 μm |
| Static sensitivity | >30 pF/g |
| *BNEA* | <100 nano-g/√Hz |
| Quality factor | <5 |
| Sensor bandwidth | 200 Hz |
| Dynamic range | 90 dB |
| Shock resistivity | >50g |
| *TNEA* | TBD |

Another limiting factor is the *CNEA* that represents the noise performance of the interface circuit. It depends on the circuit capacitive resolution and the accelerometer's sensitivity. The proposed fabrication process enables increase of the seismic mass and reduction of gap sizes, independently. *BNEA* is a function of the capacitive gap size and increases for smaller gaps. But it is improved by increasing the mass. On the other hand, sensitivity increases by reducing the gap. The optimum design specifications per unit area are achieved by increasing the mass through saving the handle-layer silicon and reducing gaps with deposited polysilicon. Figure 2.15 and 2.16 illustrate the change of the sensitivity and *BNEA* with respect to the amount of the gap reduction with polysilicon. The initial gap spacing is 9 μm and the device layer is 100 μm. Deposited polysilicon changes the tethers' thickness as well, which causes the mechanical compliance and therefore the sensitivity to first show reduction with poly deposition. A capacitive gap size greater than 4 μm satisfies the *BNEA* and *S* requirements for the target accelerometer. However, the mechanical quality factor *(Q)* should be examined to guarantee the accelerometer is stable (Figure 2.17).

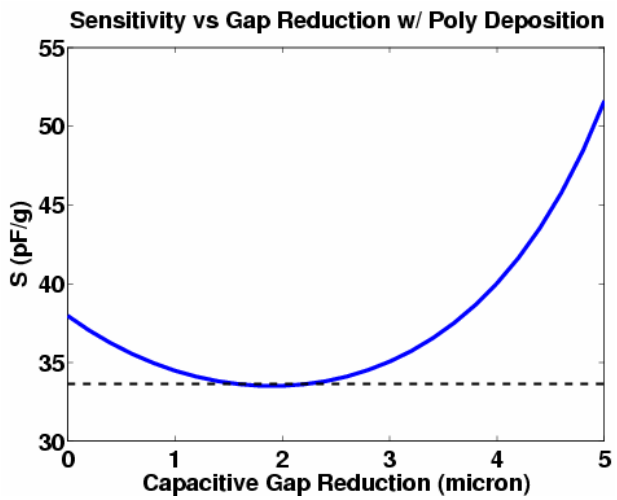



Figure 2.15: Sensitivity with respect to the gap reduction by polysilicon deposition.

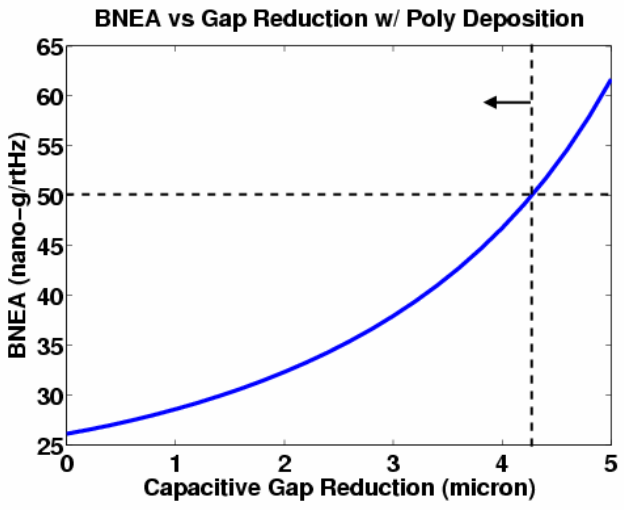



Figure 2.16: *BNEA* with respect to the gap reduction by polysilicon deposition.

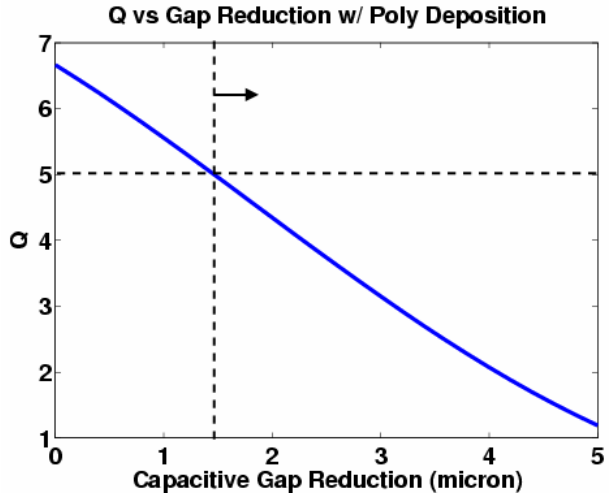



Figure 2.17: *Q*-factor with respect to the gap reduction by polysilicon deposition.

Since the seismic mass is very large (10's of milli-gram) and the accelerometer is very compliant, the device is vulnerable to damage caused by mechanical shock. Hence, shock stops and deflection limiters are devised to protect the accelerometer and avoid non-linear effects caused by momentum of the off-plane center of mass. A pitch of 60 μm is selected to place 110 electrodes in each side of the accelerometer (Figure 2.18).

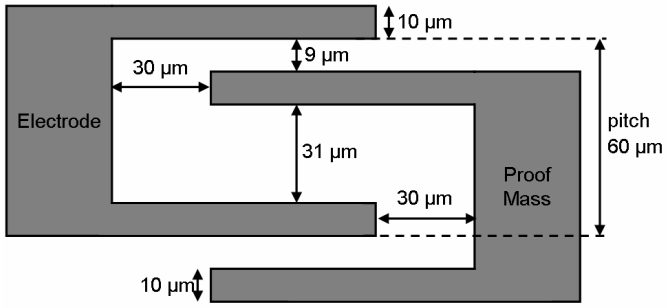



Figure 2.18: Schematic diagram of a sense electrode pitch with dimensions.

An ANSYS® simulation predicts the first mode shape (in-plane flexural) to occur at 200 Hz and the next mode shape (out-of-plane motion) to occur at 1300 Hz, which is well above the in-plane mode shape (Figure 2.19). The capacitive sensitivity to the second mode shape (torsional motion) is much smaller than the in-plane capacitive sensitivity, especially when the proof mass displacement is in the nano-meter range.

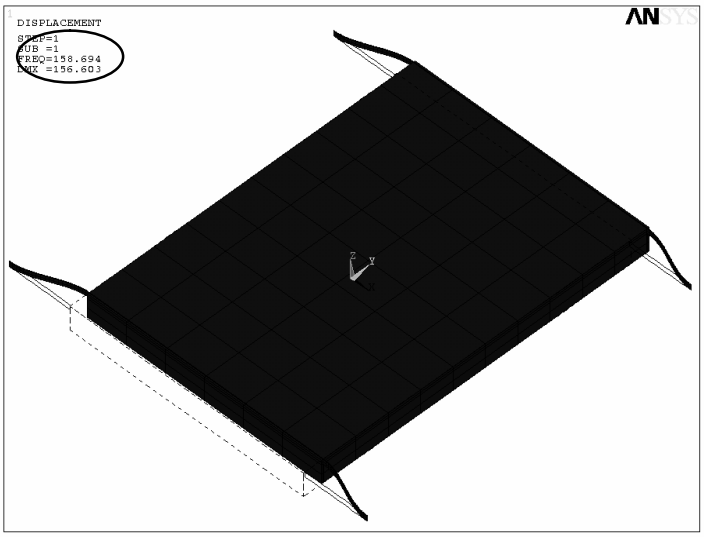



Figure 2.19: ANSYS® modal analysis of the accelerometer (in-plane motion).

### 2.4.2 FABRICATION PROCESS

Figure 2.20 illustrates the *2-mask* fabrication process flow of the sub-micro-gravity SOI accelerometer.

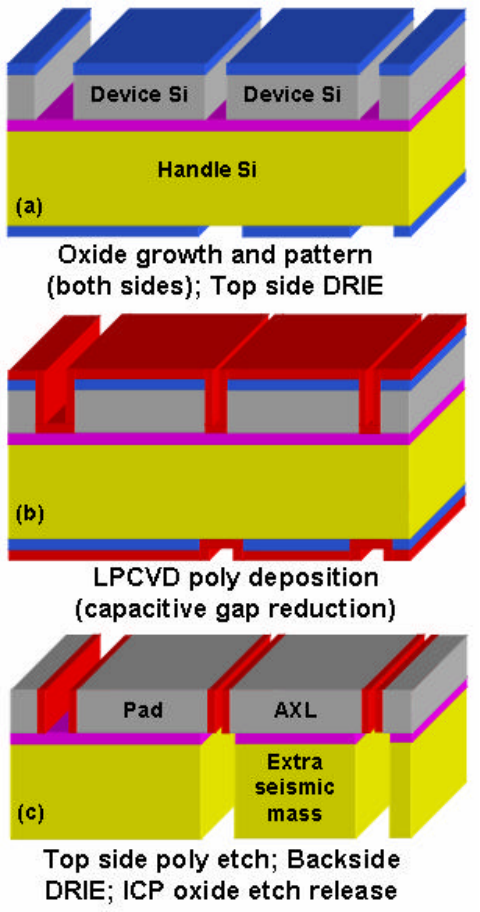



Figure 2.20: Fabrication process flow of a sub-micro-gravity SOI accelerometer.

It begins with growing a thick thermal silicon oxide on a low resistivity thick (100 μm) SOI wafer. The oxide layer is patterned on the both sides of the wafer to form the DRIE mask (Figure 2.20(a)). This will prevent further lithography step after the device layer is etched to define the accelerometer structure. Trenches are etched on the front side. A layer of LPCVD polysilicon is deposited and doped uniformly to reduce the capacitive gap size (Figure 2.20(b)). A blanket etch step removes the polysilicon at the bottom of the trenches and provides isolation between bonding pads and fingers. Then the wafer is flipped and the handle layer is etched down to the

buffer oxide (BOX) from backside. A portion of the handle silicon layer on the backside of the accelerometer's proof mass will remain intact to add substantial amount of mass. As ANSYS® predicted the accelerometer's sensitivity to the torsional motion of the off-axis proof mass is much smaller than the in-plane motion for nanometer range of proof mass displacements. At the end, the BOX is dry etched in an ICP system and the device is released (Figure 2.20(c)). In case of mounting the device on a flat packaging or testing platform, which limits the movement of accelerometer, an extra mask can be used to lower the height of the backside added mass.

The proposed fully-dry release process is key to the high-yield fabrication of extremely compliant structures with small gaps and without experiencing stiction problems. The SEM picture of a 7 mm × 7 mm microaccelerometer in 100 μm thick SOI substrate is shown in Figure 2.21. The backside of this device, showing extra seismic mass, is illustrated in Figure 2.22. The proof mass is solid with no perforation that maximizes the sensitivity and minimizes the mechanical noise floor per unit area.

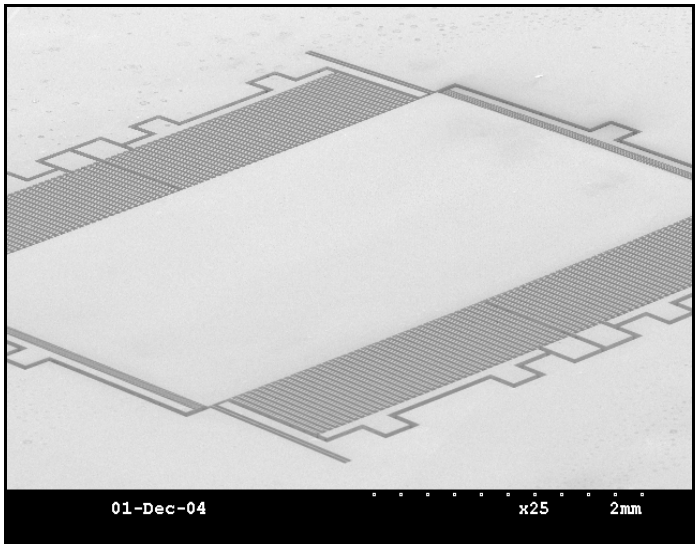



Figure 2.21: SEM picture of the accelerometer from top side.

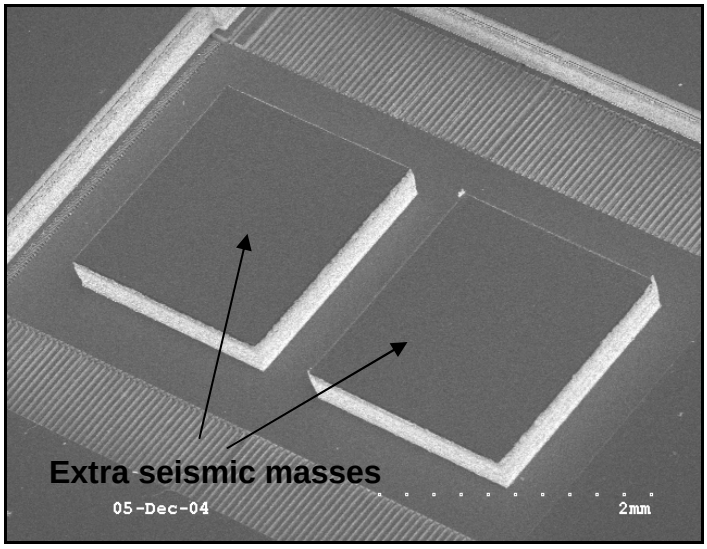



Figure 2.22: SEM picture of the backside with extra seismic masses.

A close-up view of the tether and sense electrodes is provided in Figure 2.23. While the mask opening size between readout fingers is 9 μm, the gaps are reduced to 5 μm by deposition of 2 μm polysilicon on the sidewalls (Figure 2.24).

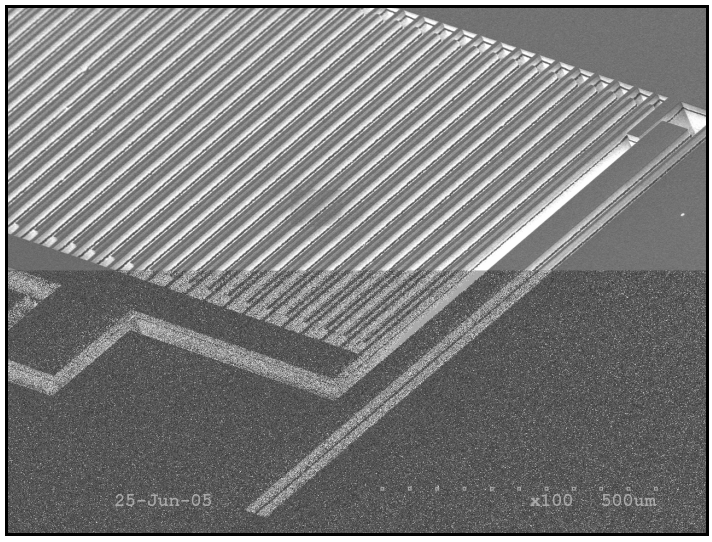



Figure 2.23: Close-up of the tether and electrodes (top view) showing no residual stress.

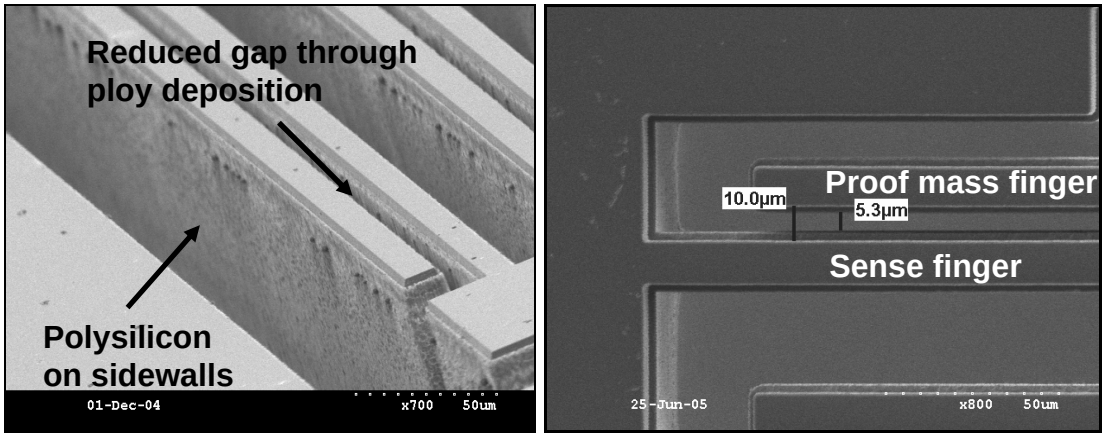



Figure 2.24: SEM pictures of reduced gaps through LPCVD polysilicon deposition.

The accelerometer is very compliant in the sense direction and its movement can cause serious damage on the sense electrodes or tethers. To protect the device, shock stops are implemented at four corners of the accelerometer. The gap between the shock stops and the proof mass is smaller than the capacitive gap that prevents the proof mass to experience large displacement. Figure 2.25 shows a close-up view of the shock absorbers.

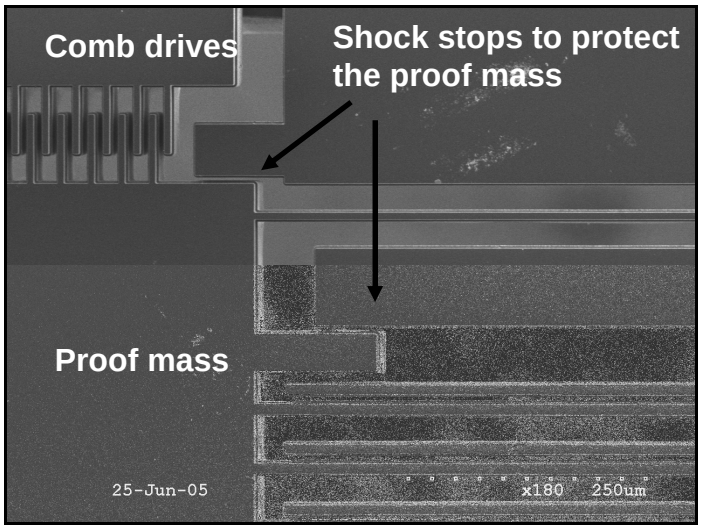
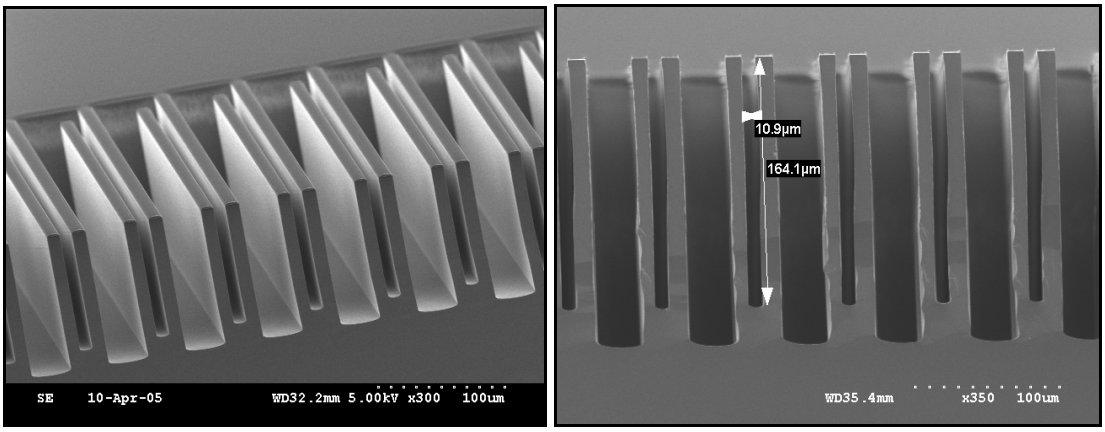



Figure 2.25: SEM picture of the implemented shock stops.

More than 5 devices were tested for the functionality and performance. They were also investigated for any residual stress caused by the LPCVD polysilicon deposition. Since the LPCVD polysilicon is symmetrically deposited over tethers in a high

temperature (600 °C), tethers are stress free. However, in one fabrication batch, we observed the residual stress and buckled tethers, which happened because of the low quality of the deposited polysilicon. It should be mentioned that LPCVD polysilicon deposition is the only high-temperature step of the process and it can be replaced with metal deposition in lower temperature to keep the process CMOS compatible. Implementation of straight DRIE trenches without footing effect and bowing in a thick SOI wafer is a very challenging task that is required to create a smooth poly deposition and to avoid non-linearity effects caused by surface roughness (Figure 2.26) [69].




(a) (b)

Figure 2.26: (a) SEM of optimized DRIE trenches; (b) Measured aspect ratio of 164:11.

The following is a list of unique features, achievable in this implementation:

- 2-mask process → High yield and simple implementation
- Fully dry release → Stiction-less compliant devices
- Gap size reduction → High capacitive sensitivity
- Small aspect ratio trenches → Relaxed DRIE requirements
- Extra backside seismic mass → Nano-gravity performance
- No release perforation (solid proof mass) → Optimized performance per unit area
- Different trench gap sizes → Effective shock stops

Design specifications of the accelerometer are summarized in Table 2.4.

Table 2.4: Design specifications of the sub-micro-gravity SOI accelerometer.

| | |
|---|---|
| Top-side proof mass<br>Extra seismic mass | 7 mm × 5 mm × 100 μm<br>6.7 mm × 4.7 mm × 400 μm |
| Overall size | 7 mm × 7 mm |
| Device thickness | 100 μm |
| Extra seismic mass thickness | 400 μm |
| Reduced capacitive gap size | 5 μm |
| Mass *(M)* | 38 milli-gram |
| Electrical Stiffness | 3.5 N/m |
| Mechanical Stiffness | 56 N/m |
| Effective Stiffness *(K)* | 52.5 N/m |
| Air squeeze-film damping *(D)* | 0.022 Ns/m |
| Quality factor *(Q)* | 2 |
| Rest capacitance *($C_S$)* | 28 pF |
| Static sensitivity | 50 pF/g |
| *BNEA* | 50 nano-g/√Hz |
| Sensor bandwidth | 200 Hz |
| Pull-in voltage | 2.6 V |
| Off-plane stiffness | 3610 N/m |

## 2.5 SUMMARY

A stiction-less MEMS fabrication process was introduced to implement capacitive micro-gravity accelerometers with solid proof masses in SOI wafers. The process flow was very simple compared to some other mixed-mode fabrication technologies that used regular silicon substrates. It consisted of two masks and only three plasma-etching steps. It was shown that for aspect-ratio-limited capacitive gaps, an optimized device thickness existed that minimized the total noise of the accelerometer system. An improved version of the fabrication process was also introduced to implement deep sub-micro-gravity capacitive SOI accelerometers in a small footprint ($<0.5cm^2$). In the new process, sensitivity of the accelerometer was increased by capacitive gap reduction through deposition of LPCVD polysilicon, and the mechanical noise floor was improved by increasing the solid seismic mass with saving some part of the handle layer attached to the proof mass. This in turn helped to effectively optimize the *TNEA*. Gap reduction technique relaxed the trench etching process and allowed for different gap sizes with higher trench aspect ratios (>20:1) to implement shock stops in thick SOI wafers. Fabricated sub-micro-gravity accelerometers were designed for a *BNEA* of 50 nano-g/√Hz and a capacitive sensitivity of 50 pF/g.

# CHAPTER 3

# ANALOG-OUTPUT MICRO-GRAVITY SOI ACCELEROMETER

## 3.1 OVERVIEW

As presented in Chapter 2, bulk micromachined SOI accelerometers provide high resolution and high sensitivity in a small form-factor. However, a thick SOI device with high trench aspect ratio increases the rest capacitance of the sensor, which puts limitations on the front-end interface circuit. Large sensor rest capacitance requires large on-chip reference capacitors to set proper input biasing of the front-end circuit. This requirement in turn limits the versatility of the designed circuit.

In this chapter, the design and implementation of a generic interface circuit for high resolution and high sensitivity capacitive SOI accelerometers is presented. In the previously reported “fully-differential” implementations, there were typically two changing capacitances with a single common node at the proof mass, requiring area-consuming on-chip reference capacitors to form a balanced capacitive bridge and set the input common mode voltage of the amplifier [70–72] (Figure 3.1).

In an effort to eliminate area-consuming on-chip reference capacitors, a new reference-capacitor-less SC charge amplifier was devised. In our architecture, the reference capacitors are absorbed in the sense capacitance of the accelerometer without compromising the sensitivity of the device or increasing area (Figure 3.2).

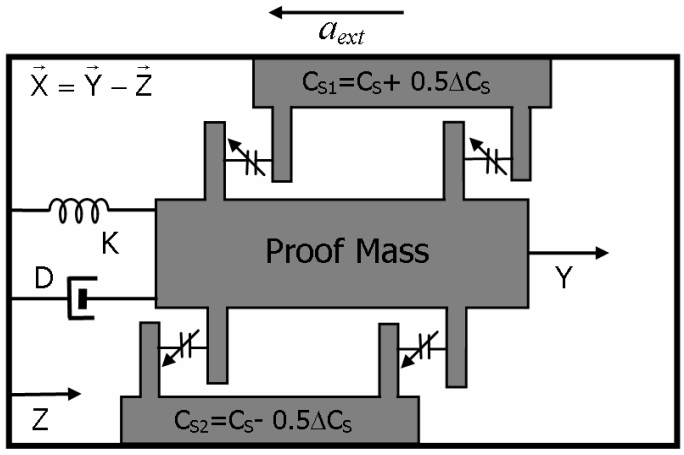



Figure 3.1: Schematic diagram of a reported capacitive microaccelerometer.

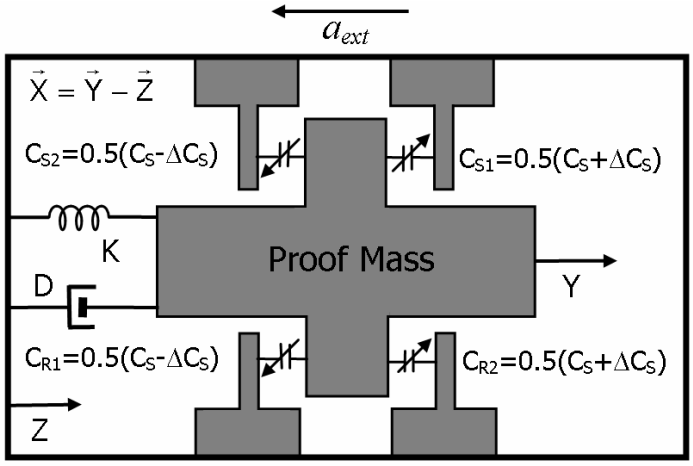



Figure 3.2: Schematic diagram of a fully-differential capacitive microaccelerometer.

At the sensor-IC interface, a switching architecture is devised such that the charge amplifier can interface with “four” changing capacitances having *one common node* at the proof mass (two increasing and two decreasing). The proof mass is tied to a DC voltage at all times and is never switched, which reduces the switching noise. The micro-gravity SOI accelerometer is fabricated through the backside dry-release process introduced in Section 2.3. The SOI accelerometer is wirebonded to the interface IC and characteristic results are obtained.

## 3.2 MICRO-GRAVITY INTERFACE CIRCUIT ARCHITECTURE

In reported implementations, the proof mass was typically switched between supply *($V_{DD}$)* and ground, which required a digital circuit capable of driving the parasitic capacitance between the proof mass and substrate [73] [74]. For bulk micromachined accelerometers, parasitic capacitors can be in the range of 10's of pF, which limit the maximum sampling clock and increase the power consumption. Figure 3.3 shows a typical front-end interface circuit for semi-differential capacitive accelerometers [74].

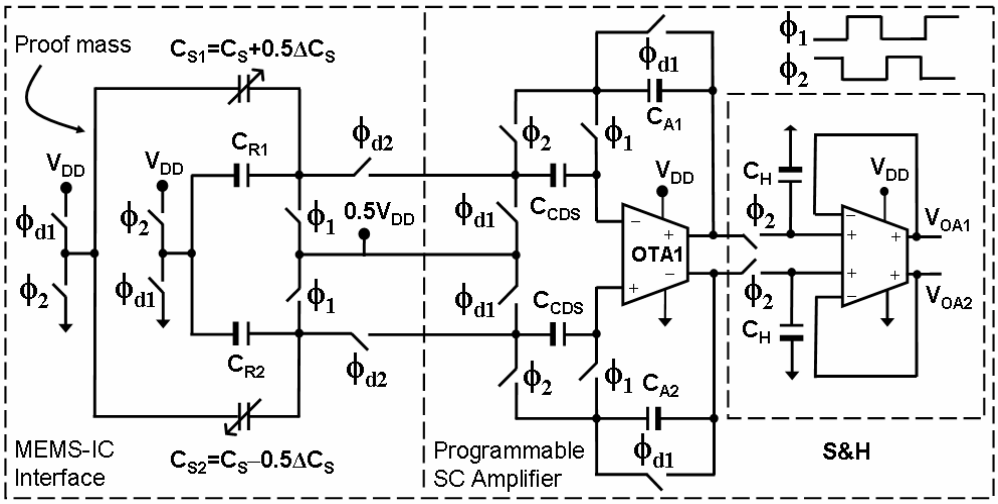



Figure 3.3: Schematic diagram of a typical front-end SC charge amplifier.

Using conservation and redistribution of charge in $C_{R1,2}$, $C_{S1,2}$ and $C_{A1,2}$ between sampling and amplification phases, one can show that the input common mode voltage *($V_{ICM}$)* of this circuit is equal to

$$V_{ICM} = 0.5\left(\frac{3C_R - C_S + C_A}{C_S + C_R + C_A}\right)V_{DD} \tag{3-1}$$

when $C_{R1}=C_{R2}=C_R$ and $C_{A1}=C_{A2}=C_A$.

For proper operation of the input amplifier, $V_{ICM}$ should remain in the common mode range. A safe value of the input common mode voltage is half of the rail *($0.5V_{DD}$)*.

$$V_{ICM} = 0.5V_{DD} \Rightarrow \frac{3C_R - C_S + C_A}{C_S + C_R + C_A} = 1 \Rightarrow C_R = C_S \tag{3-2}$$

Therefore reference capacitors should compensate for the rest capacitance of the accelerometer *($C_S$)*. It means for each accelerometer, there should be an on-chip $C_R$ such that $C_R$=$C_S$, which is the main disadvantage of this architecture. Figure 3.4 illustrates the microphotograph of the SC charge amplifier reported by the author in [74]. The IC is fabricated in the 2.5 V 0.25 µm 2-Poly 5-Metal N-well CMOS process from National Semiconductor (NSC). The core die area is 1 $mm^2$. For bulk micromachined accelerometers with large rest capacitance, a considerable portion of the die is occupied with reference capacitors (more than 50% in this implementation).

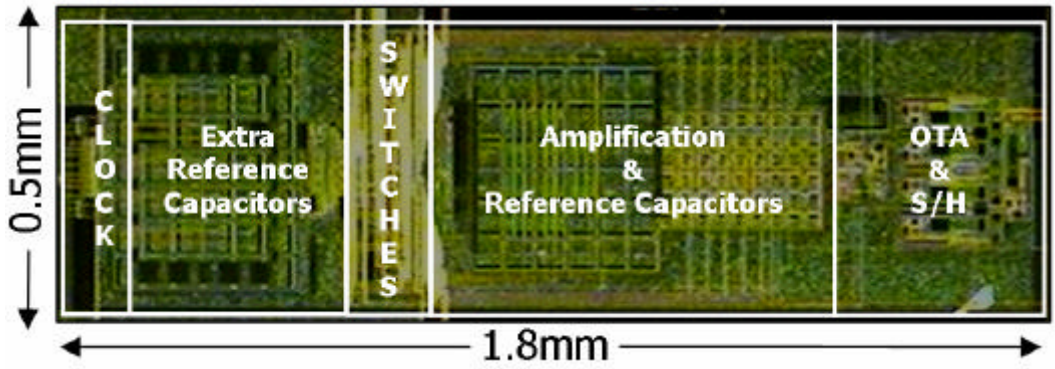



Figure 3.4: Chip microphotograph of the SC amplifier reported in [74].

### 3.2.1 Reference-Capacitor-Less SC Charge Amplifier

Figure 3.5 shows the schematic diagram of a new reference-capacitor-less front-end that consists of a fully-differential input/output SC charge amplifier followed by a sample and hold (S&H). There is no need for on-chip reference capacitors and it has the versatility of interfacing with different capacitive sensors. $C_{S1,2}$ and $C_{R1,2}$ are the accelerometer's sense capacitors; $C_{A1,2}$ are the on-chip amplification capacitors. The output common mode voltage *($V_{OCM}$)* is set to the half of the rail by the output common-mode feedback (CMFB) circuit, and the input common mode voltage *($V_{ICM}$)* is set to the half of the rail by the sensor's capacitors.

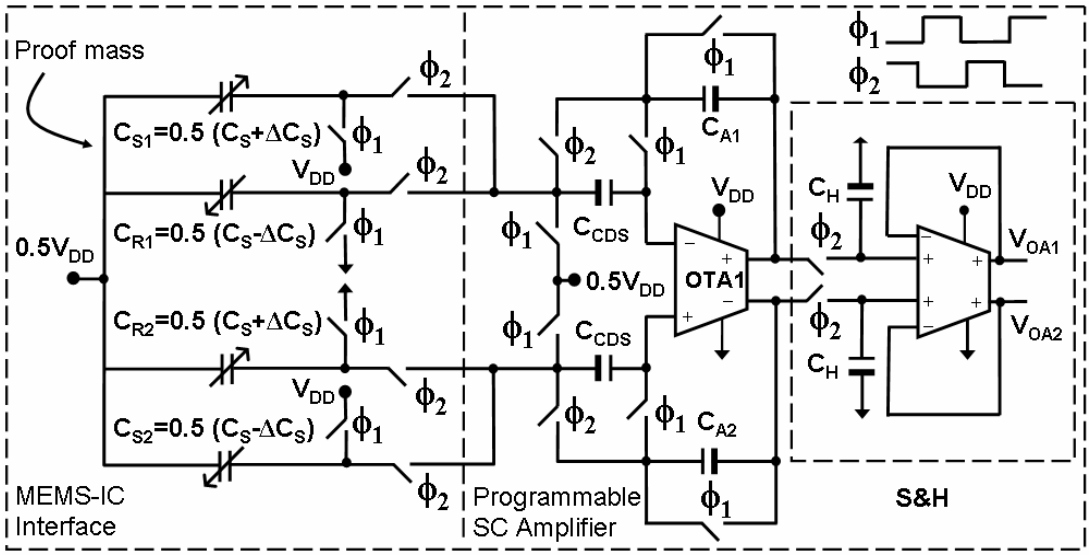



Figure 3.5: Schematic diagram of a reference-capacitor-less SC readout circuit.

The amplification capacitors are binary-weighted and are programmable through a 4-bit digital word. The fully-differential scheme helps to reduce common mode noise such as the substrate noise. Using CMOS switches, there is no need for the delayed version of the non-overlapping clocks. There are two clock phases, $f_1$ & $f_2$, involved in the circuit. In the sampling phase ($f_1$=high, $f_2$=low), $C_{S1,2}$ and $C_{R1,2}$ are charged with $0.5V_{DD}$ and amplification capacitors ($C_{A1,2}$) are discharged to zero (Figure 3.6).

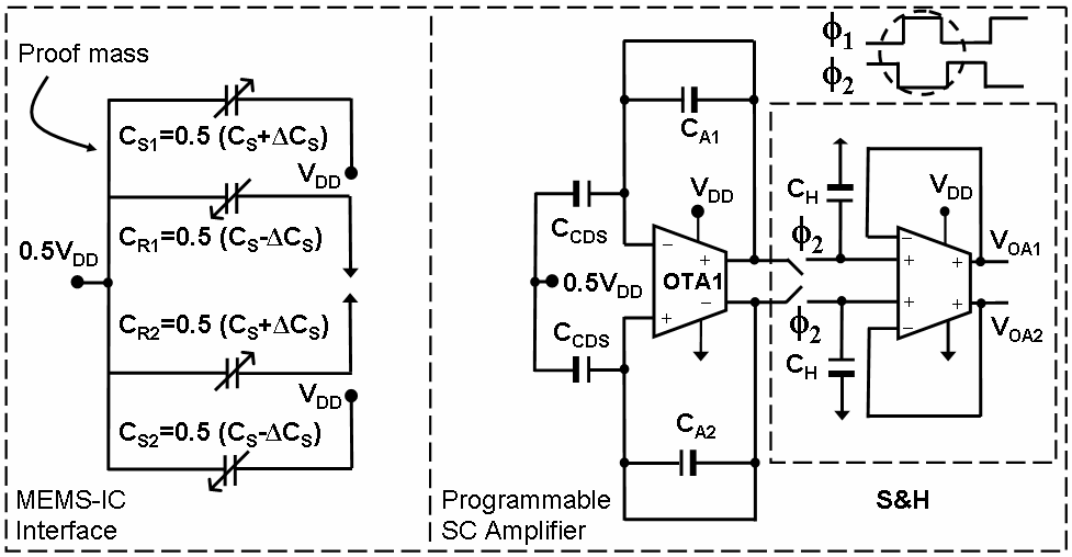



Figure 3.6: Equivalent circuit of the SC charge amplifier in the sampling phase.

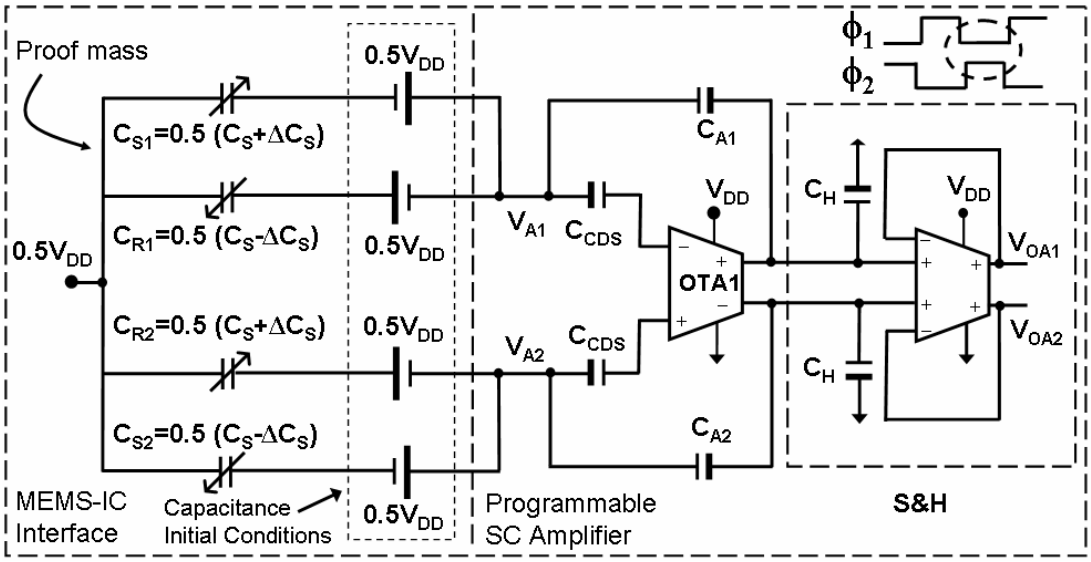



Figure 3.7: Equivalent circuit of the SC charge amplifier in the amplification phase.

Meanwhile, the correlated-double-sampling (CDS) capacitors *($C_{CDS}$)* accumulate and save the offset and instant low-frequency noises.

Figure 3.7 illustrates the amplifier in the amplification phase. In this phase *($f_1$=low, $f_2$=high*), the accumulated charge in $C_{S1,2}$ and $C_{R1,2}$ transfers to $C_{A1,2}$, and $C_{CDS}$ cancels out the slowly-changing offset and instant low-frequency noise. The use of CMOS switches helps to improve the charge injection and clock feedthrough. In addition, the elimination of the proof mass switching helps in further reduction of clock noises and improvement of the power dissipation. For simplicity, initial voltages of previously charged capacitances $C_{S1,2}$ and $C_{R1,2}$ are considered as DC voltage sources in series with the capacitors. Open-loop gain of the operational transconductance (OTA) is very large. Therefore, input nodes of the amplifier *($V_{A1}$, $V_{A2}$)* are virtual ground (isolated nodes). Following equations are obtained, using the charge redistribution from the sampling phase to the amplification phase at isolated nodes $V_{A1}$ and $V_{A2}$:

$$C_{S1}\left(V_{DD}-V_{A1}\right)-C_{R1}V_{A1}=C_{A1}\left(V_{A1}-V_{O1}\right) \tag{3-3}$$

$$C_{S2}\left(V_{DD}-V_{A2}\right)-C_{R2}V_{A2}=C_{A2}\left(V_{A2}-V_{O2}\right) \tag{3-4}$$

The effect of the virtual ground at $V_{A1}$ and $V_{A2}$ causes that $V_{A1}=V_{A2}=V_{ICM}$. Moreover, $C_{A1}=C_{A2}=C_A$, $V_{OA1}=V_{OCM}-0.5v_O$ and $V_{OA2}=V_{OCM}+0.5v_O$. Equations (3-3) and (3-4) can be arranged for differential and common mode voltages as

$$0.5\left(C_S+\Delta C_S\right)\left(V_{DD}-V_{ICM}\right)-0.5\left(C_S-\Delta C_S\right)V_{ICM}=C_A\left(V_{ICM}-V_{OCM}+0.5v_O\right) \quad (3\text{-}5)$$

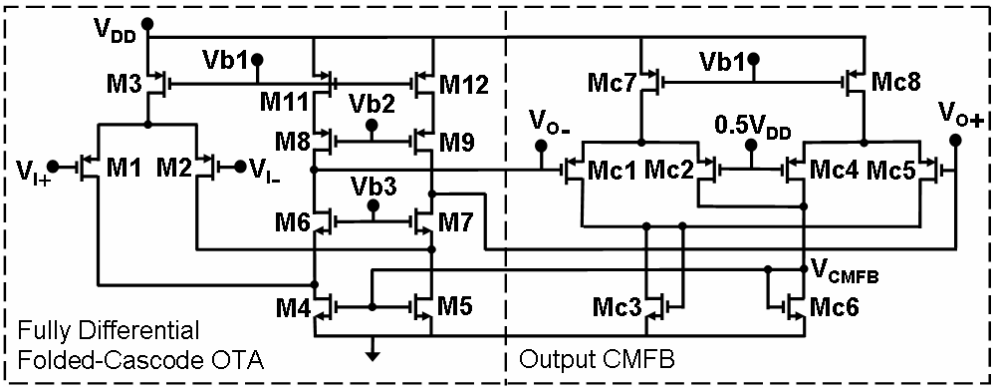
$$0.5\left(C_S-\Delta C_S\right)\left(V_{DD}-V_{ICM}\right)-0.5\left(C_S+\Delta C_S\right)V_{ICM}=C_A\left(V_{ICM}-V_{OCM}-0.5v_O\right) \quad (3\text{-}6)$$

Therefore, $V_{IMC}$ and the differential output voltage $(DV_O)$ are equal to

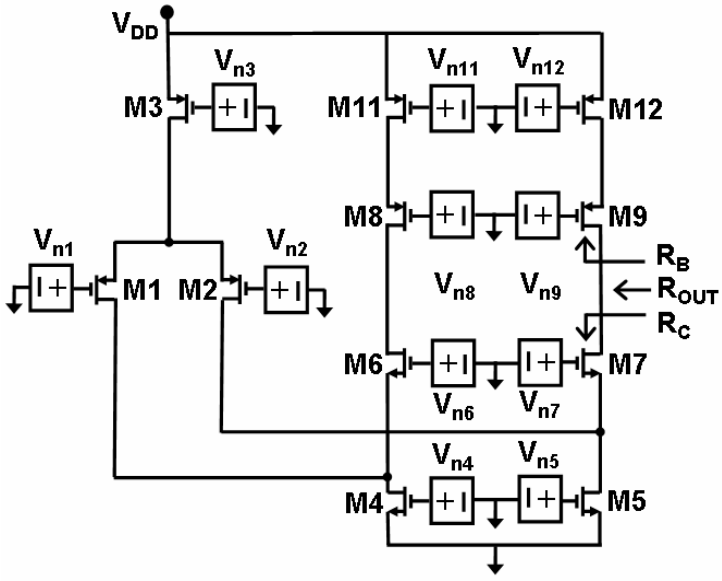
$$V_{ICM}=\frac{0.5C_SV_{DD}+C_AV_{OCM}}{C_S+C_A}=\frac{0.5C_SV_{DD}+0.5C_AV_{DD}}{C_S+C_A}=0.5V_{DD} \quad (3\text{-}7)$$

$$\Delta V_O=V_{OA1}-V_{OA2}=\frac{\Delta C_S}{C_A}V_{DD} \quad (3\text{-}8)$$

The differential output voltage is proportional to the ratio of the sense capacitance change $(DC_S)$ and programmable amplification capacitance $(C_A)$. This linear equation is later used to back-calculate the capacitive resolution of the accelerometer system from the measured output noise voltage. The S&H at the output of the front-end block acts as an impulse sampler combined with a comb filter, which interpolates subsequent sampled data and provides a smooth signal [75]. However, the S&H cannot be considered as an anti-aliasing filter (AAF) since it does not truly band-limit the output signal of the charge amplifier. Therefore, a proceeding AAF is required if a back-end Sigma-Delta (ΣΔ) analog-to-digital (A/D) converter is included [76]. The core op amp of the SC charge amplifier is a fully-differential folded-cascode OTA. Figure 3.8(a) shows the transistor level schematic of the implemented OTA, including continuous-time output common mode feedback. The OTA is self-compensated through load capacitors at the outputs. Noise model of the OTA with equivalent noise sources at the input of each transistor is shown in Figure 3.8(b).




(a)




(b)

Figure 3.8: (a) Schematic diagram of a fully-differential folded-cascode OTA; (b) Noise model of the OTA.

The differential input referred noise of the amplifier is equal to

$$\overline{V_{ni}}^2 = 2\left\{\overline{V_{n2}}^2 + \left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{V_{n4}}^2 + \left(\frac{R_B}{r_{ds2} \,||\, r_{ds4}}\right)^2 \frac{1}{\left(g_{m2}R_{out}\right)^2} \overline{V_{n6}}^2 + \left(\frac{R_c}{r_{ds10}}\right)^2 \frac{1}{\left(g_{m2}R_{out}\right)^2} \overline{V_{n8}}^2 + \left(\frac{g_{m10}}{g_{m2}}\right)^2 \overline{V_{n10}}^2\right\} \tag{3-9}$$

This equation emphasizes that transistors $M_1$, $M_2$, $M_4$, and $M_5$ contribute most of the noise. The *1/f* noise and thermal noise are the two main noise sources in the MOS transistor (Equation (3-10)). For simplicity, body effect is neglected *(h=0).*

$$\overline{V_{ni}}^2 = \left(\frac{8k_BT\left(1+h\right)}{3g_{mi}} + \frac{K_F}{C_{OX}\left(WL\right)_i}\frac{1}{f}\right) \cong \left(\frac{8k_BT}{3g_{mi}} + \frac{K_F}{C_{OX}\left(WL\right)_i}\frac{1}{f}\right) \tag{3-10}$$

As a result, the input referred noise of the fully-differential OTA is defined as

$$\frac{\overline{V_{ni}}^2}{\Delta f} \cong 2\frac{\overline{V_{n2}}^2}{\Delta f} + 2\left(\frac{g_{m4}}{g_{m2}}\right)^2 \frac{\overline{V_{n4}}^2}{\Delta f} = \frac{16k_BT}{3g_{m2}} + \frac{2K_{FPMOS}}{C_{OX}W_2L_2}\frac{1}{f} + \frac{g_{m4}}{g_{m2}^2}\frac{16k_BT}{3} + \left(\frac{g_{m4}}{g_{m2}}\right)^2 \frac{2K_{FNMOS}}{C_{OX}W_4L_4}\frac{1}{f} \tag{3-11}$$

$$\frac{\overline{V_{ni}}^2}{\Delta f} = \frac{16k_BT}{3\sqrt{2K_2'\left(\frac{W_2}{L_2}\right)I_2}} + \frac{2K_{FPMOS}}{C_{OX}W_2L_2}\frac{1}{f} + \frac{\sqrt{2K_4'\left(\frac{W_4}{L_4}\right)I_4}}{2K_2'\left(\frac{W_2}{L_2}\right)I_2}\frac{16k_BT}{3} + \frac{K_4'L_2I_4}{K_2'W_2I_2}\frac{2K_{FNMOS}}{C_{OX}L_4^2}\frac{1}{f} \tag{3-12}$$

Large area PMOS transistors *($M_1$, $M_2$)* are used at the input stage to reduce the inherent flicker noise of the OTA. The transconductance *($g_m$)* of the input transistors are large to avoid noise contributions of other transistors. Also, the lengths of the load transistors *($M_4$, $M_5$)* are larger than the lengths of the input transistors to minimize the noise contribution of the load transistors. The CMFB includes a continuous-time differential averaging amplifier (DAA), which makes it possible to test the OTA block, separately. The biasing voltages are generated from a bootstrapped current source.

## 3.3 OFFSET AND LOW-FREQUENCY NOISE IN SC AMPLIFIERS

Voltage amplification is one of the most common functions in analog signal processing. The schematic diagram of a non-inverting SC amplifier, most often used in discrete-time signal processing, is shown in Figure 3.9.

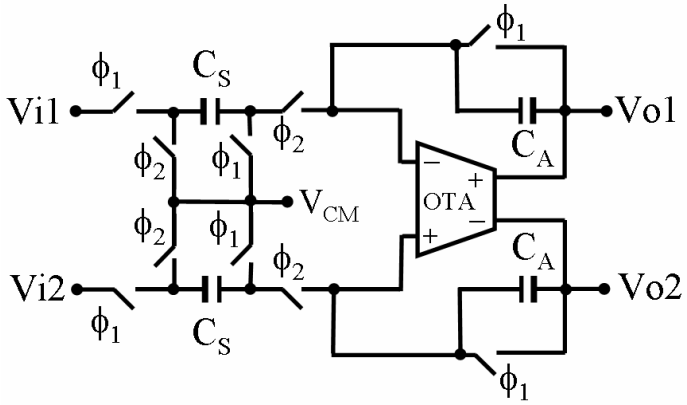



Figure 3.9: A fully-differential non-inverting SC voltage amplifier.

The input-output relation of this circuit is simply as

$$\frac{V_O(z)}{V_i(z)} = \frac{C_S}{C_A} z^{-0.5} \tag{3-13}$$

The main disadvantage of SC circuits is that the offset voltage and the input-referred noise of the op amp affect the output voltage. Denoting the input offset and input-referred low-frequency noise by $V_{OST}$, the equivalent circuit of Figure 3.10 can be used to represent the effect.

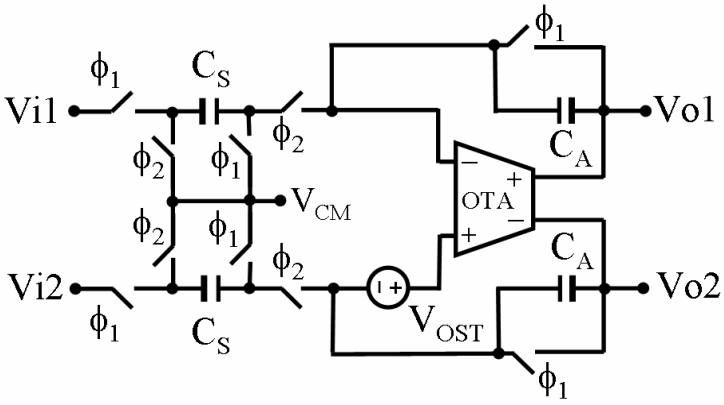



Figure 3.10: Modeling the offset and low-frequency noise in an SC amplifier.

The gain of the amplifier for the offset and low-frequency noise is [77]

$$\frac{V_O(z)}{V_{OST}(z)} = \left(1 + \frac{C_S}{C_A}\right) \tag{3-14}$$

As an example, for a gain of 10 and an offset voltage of 10 mV, the output voltage is 0.11V and this value can change significantly with the temperature and time, which is not acceptable in many applications. To reduce the effects of the op amp offset and low-frequency noise, correlated-double-sampling (CDS) scheme is used. Figure 3.11 shows the non-inverting SC voltage amplifier with the CDS circuit.

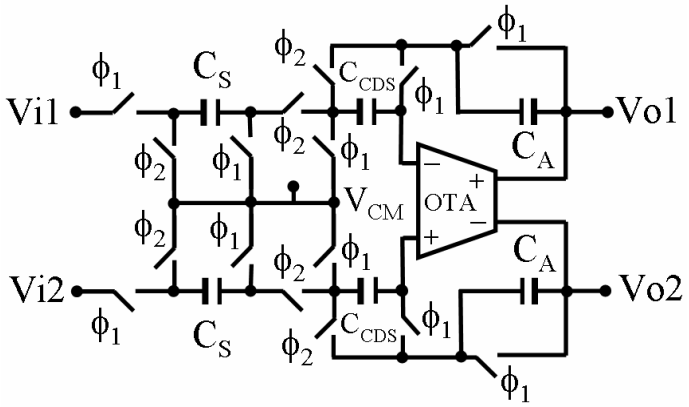



Figure 3.11: A fully-differential SC amplifier with CDS scheme.

For simplicity, a single input-output equivalent circuit is considered (Figure 3.12).

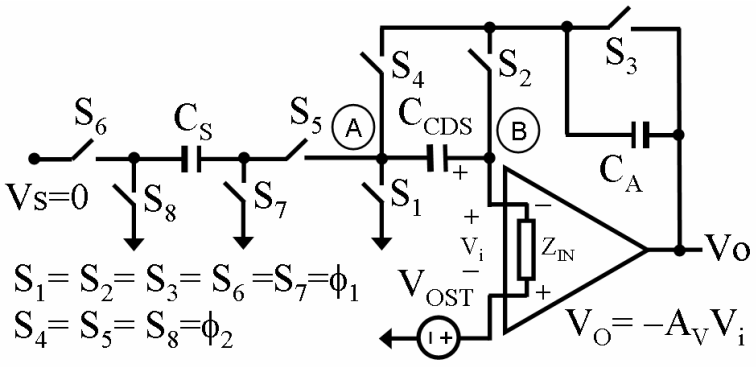



Figure 3.12: Single input-output SC amplifier with CDS scheme.

In the ideal case, where $Z_{IN} \rightarrow \mu$ and $A_V \rightarrow \mu$, the *Z*-domain noise transfer function *(NTF)* of the offset at the virtual input of the amplifier (node *A*) is equal to

$$V_A(z) = \left(1 - z^{0.5}\right) V_{OST}(z) \Rightarrow NTF(z) = \frac{V_A(z)}{V_{OST}(z)} = \left(1 - z^{0.5}\right) \qquad (3\text{-}15)$$

This equation explains that the offset (regardless of the value of the $C_{CDS}$) is cancelled since there is a null at DC, and also the low-frequency noise is high passed through the noise transfer function. However, real measurement of the CDS effect shows that the amount of the low-frequency noise cancellation depends on the value of the CDS capacitor [74] [78] [79]. In the following section, an analytical method is presented to predict the effect of the CDS capacitor in low-frequency noise cancellation when non-idealities, such as finite op amp gain, finite input impedance, and on-resistance of CMOS switches, are come to account.

### 3.3.1 CDS MODELING IN SC VOLTAGE AMPLIFIERS

In this method, the equivalent circuit of the amplifier in each consecutive sampling and amplification phases is considered, and the continuous-time noise transfer function (NTF) from the input offset source to the virtual ground at the input of the amplifier is derived. The overall noise transfer function for each consecutive sampling and amplification phases is equal to the subtraction of the transfer functions derived in each phase [80] [81]. Figure 3.13 shows the equivalent circuit of the non-inverting SC amplifier during the sampling phase *($f_1$ = high, $f_2$ = low)*. $R_i$ denotes the series resistance of the *ith* switch when it is on. The off-resistance of switches is considered infinity.

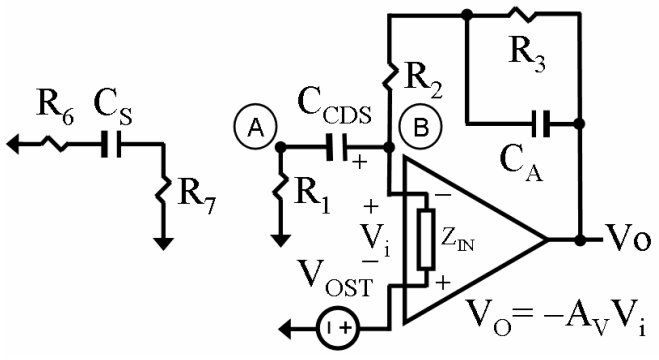



Figure 3.13: Equivalent circuit of an SC amplifier in the sampling phase.

Writing KCL at node *B*, one can find following equations:

$$\frac{V_B - V_{OST}}{Z_{IN}} + \frac{sC_{CDS}}{1+sC_{CDS}R_1}V_B + \frac{V_B - V_O}{R_2 + R_3} = 0 \tag{3-16}$$

$$V_O = -A_V\left(V_B - V_{OST}\right) \tag{3-17}$$

The first noise transfer function from the amplifier's offset to the virtual input of the amplifier (node *B*) is equal to

$$NTF_1(s) = \frac{V_B}{V_{OST}} = \frac{\dfrac{1}{Z_{IN}} + \dfrac{A_V}{R_2 + R_3}}{\dfrac{1}{Z_{IN}} + \dfrac{sC_{CDS}}{1+SC_{CDS}R_1} + \dfrac{(1+A_V)}{R_2 + R_3}} \tag{3-18}$$

This noise transfer function ($NTF_1$) is no longer independent of the CDS capacitor. It only converges to 1 when $A_V$ and $Z_{IN}$ go to infinity. In this equation, the effect of $C_A$ is neglected since $R_3$ ($R_{ON}$ of the *S3*) is much smaller than $1/sC_A$, especially in low frequencies. Figure 3.14 shows the equivalent circuit in the amplification phase.

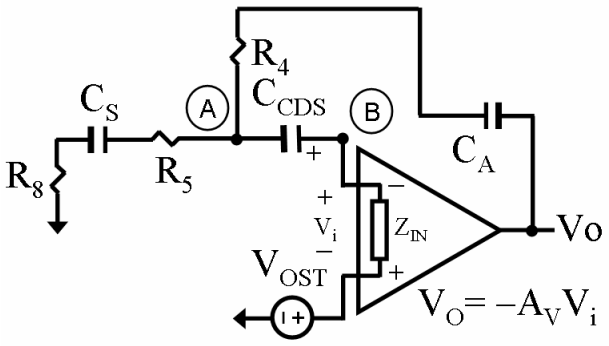



Figure 3.14: Equivalent circuit of an SC amplifier in the amplification phase.

Again with KCL at node *A*, one can find following equations:

$$\frac{sC_S}{1+sC_S\left(R_5+R_8\right)}V_A+\frac{sC_{CDS}}{1+sC_{CDS}Z_{IN}}\left(V_A-V_{OST}\right)+\frac{sC_A}{1+sC_AR_4}\left(V_A-V_{OST}\right)=0 \qquad (3\text{-}19)$$

$$V_O=\frac{sC_{CDS}A_V}{1+SC_{CDS}Z_{IN}}\left(V_A-V_{OST}\right) \qquad (3\text{-}20)$$

As a result, the second noise transfer function from the input offset source to the virtual input of the amplifier (node *A*) is equal to

$$NTF_2\left(s\right)=\frac{V_A\left(s\right)}{V_{OST}\left(s\right)}=\frac{\frac{C_{CDS}}{1+sC_{CDS}R_{IN}}\left(1+\frac{sC_AA_V}{1+sC_AR_4}\right)}{\frac{C_S}{1+sC_S\left(R_5+R_8\right)}+\frac{C_A}{1+sC_AR_4}+\frac{C_{CDS}}{1+sC_{CDS}R_{IN}}\left(1+\frac{sC_AA_V}{1+sC_AR_4}\right)} \qquad (3\text{-}21)$$

The limit of $NTF_2$, for $A_V$ and $Z_{IN}\rightarrow$ ¥, is also 1. Since the circuit should be evaluated in both the sampling and amplification phases, the effect of each noise transfer function on the instant slowly-varying offset and low-frequency noise is included in the overall noise transfer function as below:

$$NTF\left(s\right)=NTF_1\left(s\right)-NTF_2\left(s\right) \qquad (3\text{-}22)$$

The DC gain of the *NTF* is equal to

$$\left|NTF\left(0\right)\right|=\frac{\frac{1}{R_{IN}}+\frac{A_V}{R_2+R_3}}{\frac{1}{R_{IN}}+\frac{\left(1+A_V\right)}{R_2+R_3}}-\frac{C_{CDS}}{C_S+C_A+C_{CDS}}\cong\frac{C_S+C_A}{C_S+C_A+C_{CDS}} \qquad (3\text{-}23)$$

This equation suggests that the CDS capacitor should be large to improve the offset and low-frequency noise cancellation. Also, the use of fully-differential architecture helps in further suppression of the instant offset and low-frequency noise. In an SC charge amplifier, $C_S$ represents the accelerometer's sense capacitor. MATLAB

simulation was used to plot the frequency response of the overall noise transfer function for different CDS capacitors (with an amplifier's DC gain of 70 dB and input impedance of 100 MΩ). On-resistance of the CMOS switches was considered 10 kΩ. Figure 3.15 shows the simulation results. It is predicted that offset and low-frequency noise are suppressed better when the CDS capacitor is larger.

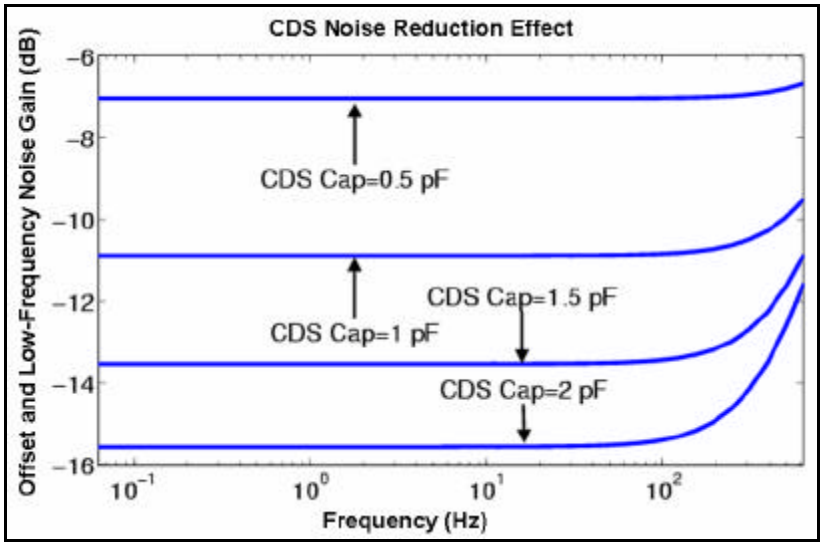



Figure 3.15: CDS simulation results for different CDS capacitors.

The accuracy of the presented model is evaluated through real measurement data that are provided in Chapter 4 and Chapter 5 [76] [79].

## 3.4 THERMAL NOISE ANALYSIS OF SC VOLTAGE AMPLIFIERS

In Figure 3.5, transmission gates (TGs) are used to implement the CMOS switches. Although, charge injection and clock feedthrough are improved by using CMOS switches and the proceeding low-pass filter at the output but non-zero resistances of the CMOS switches generate wide-band thermal noise [82]. Figure 3.16 shows the simplified noise model of the SC amplifier in the amplification phase including thermal noise sources of the on-switches.

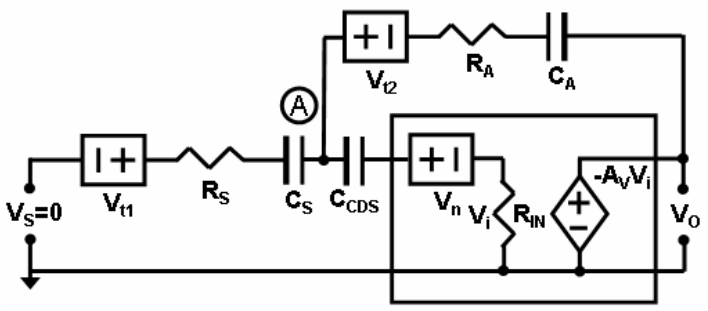



Figure 3.16: Simplified noise model of the SC amplifier in the amplification phase.

$V_n$ is the input referred noise of the OTA; $V_{t1}$ and $V_{t2}$ are the thermal noises of $R_S$ and $R_A$. Figure 3.17 shows the equivalent circuit for a noise-less amplifier.

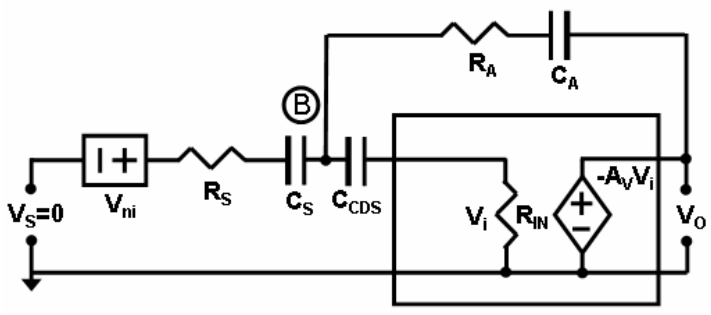



Figure 3.17: Equivalent circuit for a noise-less amplifier.

$V_{ni}$ is the total input referred noise. By writing KCL at nodes *A* and *B* and finding the output voltage for each of the circuits, the total input referred noise is calculated as follow:

*KCL at node A:* $$\frac{sC_S\left(V_{t1}-V_A\right)}{1+sC_SR_S}+\frac{sC_A\left(V_{t2}+V_O-V_A\right)}{1+sC_AR_A}+\frac{sC_{CDS}\left(V_n-V_A\right)}{1+sC_{CDS}R_{IN}}=0 \tag{3-24}$$

$$V_A=V_n-\frac{1+sC_{CDS}R_{IN}}{A_VR_{IN}sC_{CDS}}V_O \tag{3-25}$$

Therefore,

$$\begin{aligned}V_O&\left\{\frac{C_S\left(1+sC_{CDS}R_{IN}\right)}{A_VR_{IN}C_{CDS}\left(1+sC_SR_S\right)}+\frac{C_A\left(1+sC_{CDS}R_{IN}\right)}{A_VR_{IN}C_{CDS}\left(1+sC_AR_A\right)}+\frac{sC_A}{1+sC_AR_A}+\frac{1}{A_VR_{IN}}\right\}\\&=\left(\frac{sC_S}{1+sC_SR_S}+\frac{sC_A}{1+sC_AR_A}\right)V_n-\frac{sC_S}{1+sC_SR_S}V_{t1}-\frac{sC_A}{1+sC_AR_A}V_{t2}\end{aligned} \tag{3-26}$$

For large op amp gain *($A_V$)*, large CMOS input resistance *($R_{IN}$)* and low sensor bandwidth (<2 kHz), Equation (3-26) is simplified to

$$V_O\left(s\right)=\left(\frac{C_S}{C_A}\frac{1+sC_AR_A}{1+sC_SR_S}+1\right)V_n-\frac{C_S}{C_A}\frac{1+sC_AR_A}{1+sC_SR_S}V_{t1}-V_{t2} \tag{3-27}$$

*KCL at node B:* $$\frac{sC_S\left(V_{ni}-V_B\right)}{1+sC_SR_S}+\frac{V_O}{A_VR_{IN}}+\frac{sC_A\left(V_O-V_B\right)}{1+sC_AR_A}=0 \tag{3-28}$$

$$V_B=-\frac{1+sC_{CDS}R_{IN}}{A_VR_{IN}sC_{CDS}}V_O \tag{3-29}$$

Again for large $A_V$ and $R_{IN}$, the output voltage is equal to

$$V_O\left(s\right)=-\frac{C_S}{C_A}\frac{1+sC_AR_A}{1+sC_SR_S}V_{ni} \tag{3-30}$$

The input referred voltage noise is then:

$$V_{ni}\left(s\right)=-\left(\frac{C_A}{C_S}\frac{1+sC_SR_S}{1+sC_AR_A}+1\right)V_n+V_{t1}+\frac{C_A}{C_S}\frac{1+sC_SR_S}{1+sC_AR_A}V_{t2} \tag{3-31}$$

and the input referred noise power spectrum is

$$\frac{\overline{V}_{ni}^2(w)}{\Delta f}=\frac{V_{ni}(jw)V_{ni}^*(jw)}{\Delta f}=\left\{1+\frac{2C_A}{C_S}\frac{1+w^2C_SR_SC_AR_A}{1+(wC_AR_A)^2}+\left(\frac{C_A}{C_S}\right)^2\frac{1+(wC_SR_S)^2}{1+(wC_AR_A)^2}\right\}\frac{\overline{V}_n^2(w)}{\Delta f}$$
$$+\frac{\overline{V}_{t1}^2(w)}{\Delta f}+\left(\frac{C_A}{C_S}\right)^2\frac{1+(wC_SR_S)^2}{1+(wC_AR_A)^2}\frac{\overline{V}_{t2}^2(w)}{\Delta f} \tag{3-32}$$

For the designed SC amplifier, the CDS scheme suppresses the offset and low-frequency noise of the amplifier. Therefore, the op amp noise is dominated with the thermal noise of the input PMOS transistors.

$$\overline{V}_n^{\,2}=\frac{16k_BT}{3g_{m1}}\Delta f \tag{3-33}$$

$$\overline{V}_{t1}^{\,2}=4k_BTR_S\Delta f \tag{3-34}$$

$$\overline{V}_{t2}^{\,2}=4k_BTR_A\Delta f \tag{3-35}$$

$$\frac{\overline{V}_{ni}^2(f)}{\Delta f}=\left\{1+\frac{2C_A}{C_S}\frac{1+(2p\,f)^2C_SR_SC_AR_A}{1+(2p\,fC_AR_A)^2}+\left(\frac{C_A}{C_S}\right)^2\frac{1+(2p\,fC_SR_S)^2}{1+(2p\,fC_AR_A)^2}\right\}\frac{16k_BT}{3g_{m1}}$$
$$+4k_BTR_S+\left(\frac{C_A}{C_S}\right)^2\frac{1+(wC_SR_S)^2}{1+(wC_AR_A)^2}4k_BTR_A \tag{3-36}$$

Equation (3-36) suggests that one should reduce the on-resistance of the CMOS switches, reduce $C_A$ and increase $C_S$ to minimize the thermal noise contribution of the switches. For $C_S$=$C_A$ and $R_S$=$R_A$=$R_{ON}$, the input referred noise is

$$\frac{\overline{V}_{ni}^{\,2}}{\Delta f}=\frac{64k_BT}{3g_{m1}}+8k_BTR_{ON} \tag{3-37}$$

In the charge amplifier, $C_S$ is the rest capacitance of the microaccelerometer, and $C_A$ is the programmable amplification capacitor. As provided in Equation (3-37), the input referred noise is still wide-band and it can be band-limited through the S&H and proceeding low-pass filters.

## 3.5 MICRO-GRAVITY ACCELEROMETER-IC TEST RESULTS

Transistor-level simulation of the designed interface circuit was performed using Spectre® in Cadence, and time varying capacitances (representing the accelerometer's sense capacitors) were modeled using Verilog-A. A 2.5 V 0.25 μm 2-Poly 5-Metal N-well CMOS process from National Semiconductor (NSC) was provided to implement the IC chip. Virtuoso® was used to draw the MEMS and IC layouts. To minimize the implementation errors, a complete design and evaluation cycle, including parasitic extraction and layout-versus-schematic (LVS) comparison, was carried out before each IC submission. The core op amp was first designed and implemented. As a result of using a continuous-time CMFB, it was possible to test the OTA block separately for the frequency response, slew rate and noise performance. Table 3.1 demonstrates the OTA design specifications.

Table 3.1: Design specifications of a fully-differential folded-cascode OTA.

| | |
|---|---|
| Power supply | 2.5 V-GND |
| Current consumption | 150 μA |
| Open-loop DC gain *($A_{V0}$)* | 70 dB |
| Unity gain bandwidth *(GBW)* | 5.5 MHZ for $C_L$=5 pF |
| Phase margin *(PM)* | >60° for $C_L$=5 pF |
| Input common-mode rejection ratio *(ICMRR)* | 70 dB |
| Input common-mode voltage range *($V_{ICR}$)* | 0 to 2 V |
| Output common-mode voltage *($V_{OCM}$)* | 1.25 V |
| Max. differential output swing | 2.5 V |
| Input referred noise | 10 μV (f=0.1 to 100 Hz) |

The simulated frequency response of the OTA with a capacitive load of 5 pF is provided in Figure 3.18.

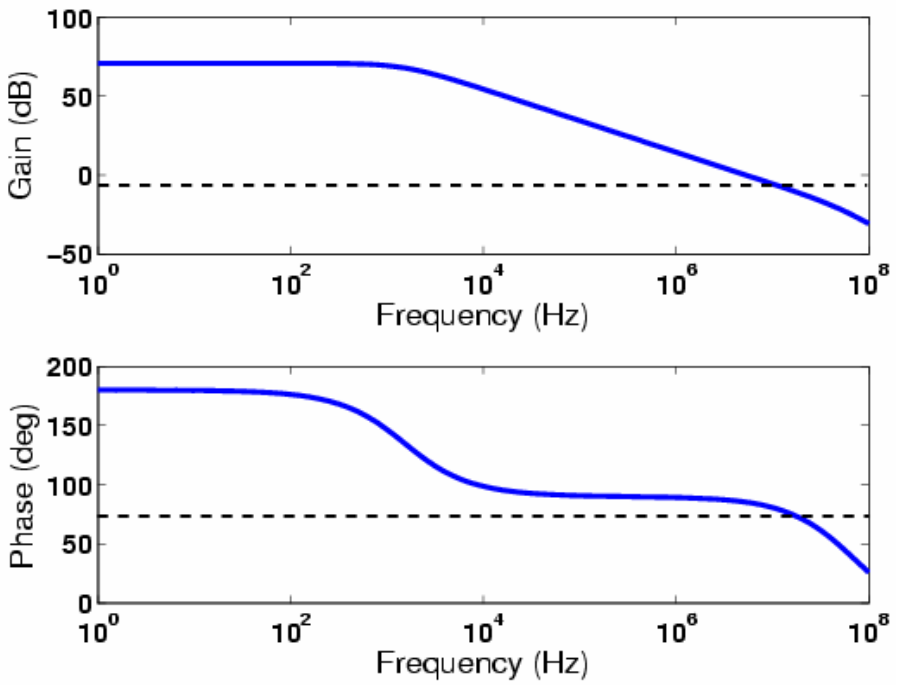



Figure 3.18: Simulated frequency response of the differential folded-cascode OTA.

The OTA has a simulated open-loop DC gain of 70 dB and a unity gain-bandwidth (GBW) of 5.5 MHz with a phase margin (PM) of 66°.

Figure 3.19 illustrates the test setup to measure the frequency response and noise performance of the designed OTA. The use of an *RC* network in the feedback loop provides the bias stability of the op amp.

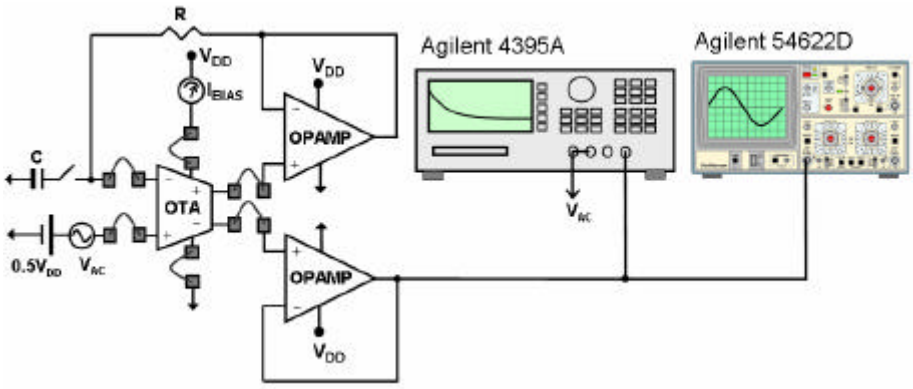



Figure 3.19: Test setup to measure the OTA frequency response and noise.

Figure 3.20 shows the picture of a custom-designed printed-circuit board (PCB) used to measure the OTA performance.

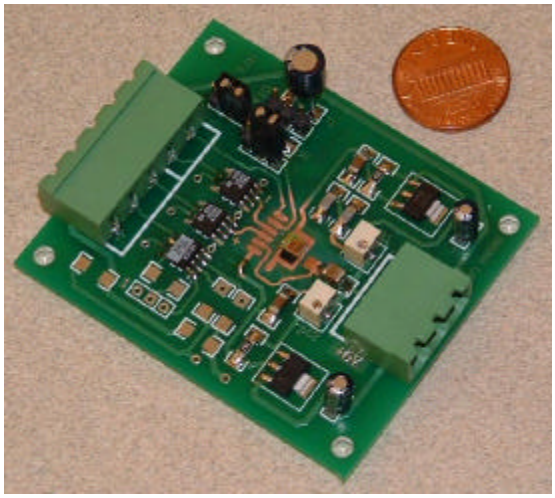
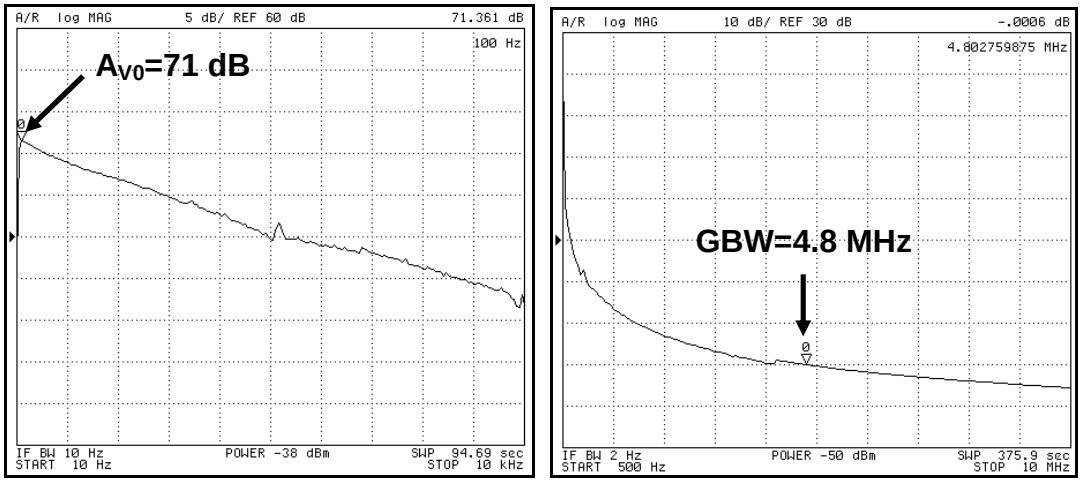


Figure 3.20: Custom-designed OTA test board.

The OTA has a measured open-loop gain of 71 dB and a measured *GBW* of 4.8 MHz (Figure 3.21). The current consumption is 160 μA with a power supply of 2.5 V.

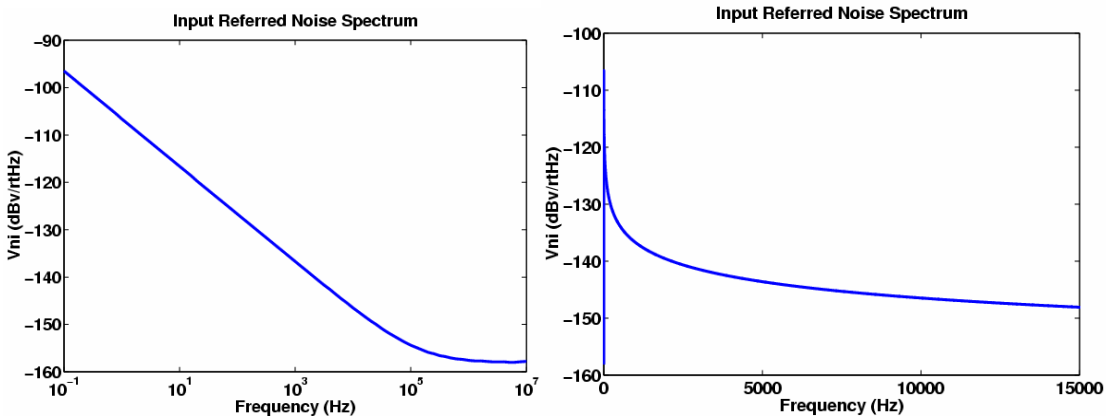



(a) (b)

Figure 3.21: Measured frequency response of the fully-differential folded-cascode OTA; (a) DC gain; (b) Unity gain bandwidth.

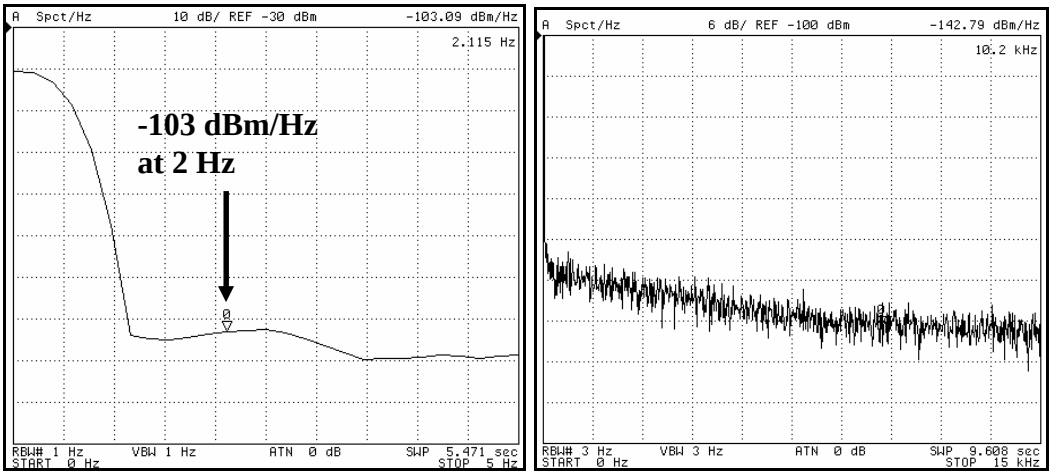
Figure 3.22 shows the noise simulation of the OTA in a unity gain configuration. The core op amp was designed for the optimized noise performance. Moreover, fully-differential scheme helps to suppress the instant common-mode interferences. The simulated input referred noise $(V_{ni})$ is 10 μV (100 dBV) in a *BW* of 0.1 to 100 Hz. The measured noise power is -103 dBm/Hz at 2 Hz with a resolution bandwidth (RBW) of

1 Hz (equivalent to -113 dBV/√Hz) and -143 dBm/Hz at 10 kHz with a RBW of 3 Hz (Figure 3.23). The measured noise performance is in a good agreement with the simulation results.




(a) (b)

Figure 3.22: Simulated input referred noise (a) Logarithmic scale; (b) Linear scale.




(a) (b)

Figure 3.23: (a) Output low-frequency noise; (b) Output noise from 0 to 15 kHz.

This OTA was used in the SC charge amplifier. The amplifier was simulated for a peak capacitive change of 0.4 pF at 75 Hz with an amplification capacitance of 1 pF and a sampling clock frequency of 500 kHz. Differential output voltages before and after the S&H and an extra low-pass filter are provided in Figure 3.24.

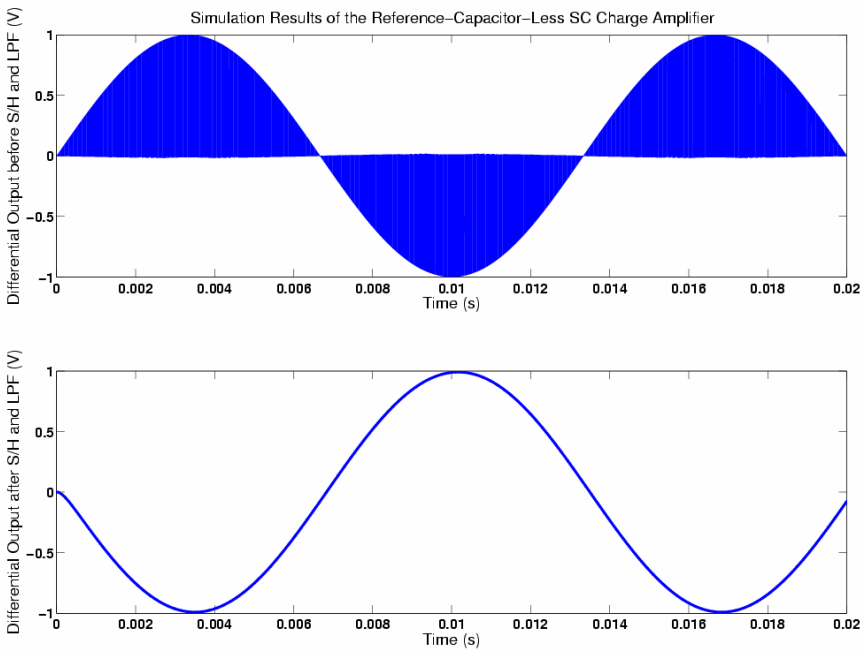



Figure 3.24: Simulated outputs of the SC amplifier ($DC_S$=0.4 pF at 75 Hz).

The use of S&H helps smooth the output voltage and filter high frequency components. The chip microphotograph is shown in Figure 3.25. The IC has a core area of 0.2 $mm^2$ and is fabricated in the 2.5 V 0.25µm 2P5M N-well CMOS process from NSC.

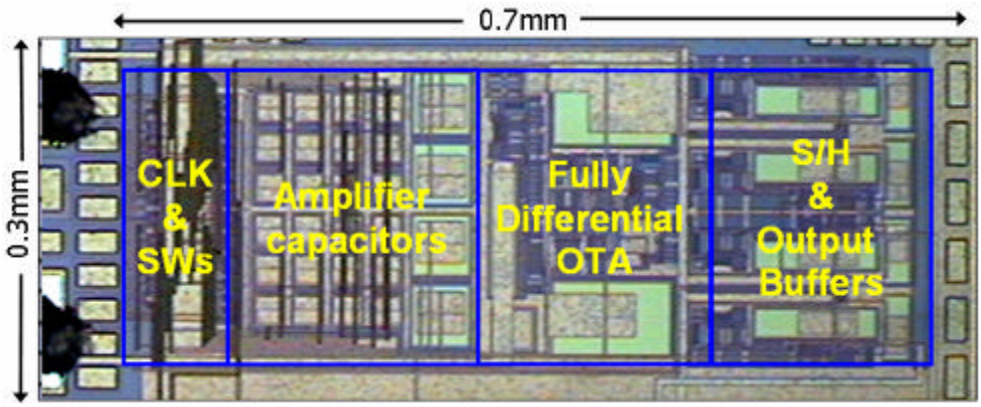



Figure 3.25: Chip microphotograph.

A significant die size reduction of 75% was achieved through the use of a reference-capacitor-less SC charge amplifier. Figure 3.26 illustrates the measured differential output.

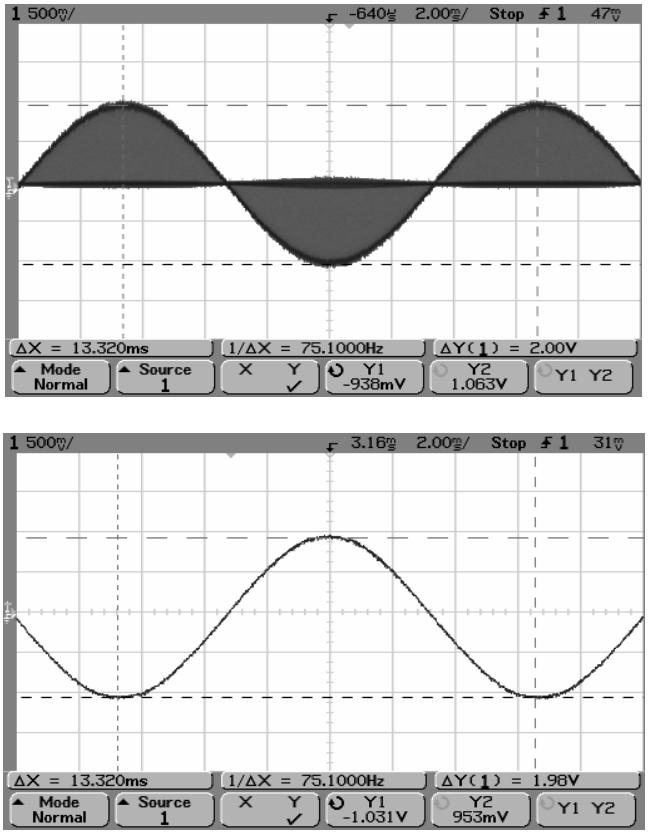



Figure 3.26: Measured differential output before and after the S&H and external low-pass filter.

Simulation results of the input common-mode voltage are provided in Figure 3.27. It is verified that $V_{ICM}$ is automatically set at $0.5V_{DD}=1.25\ V$ through the measured data (Figure 3.28).

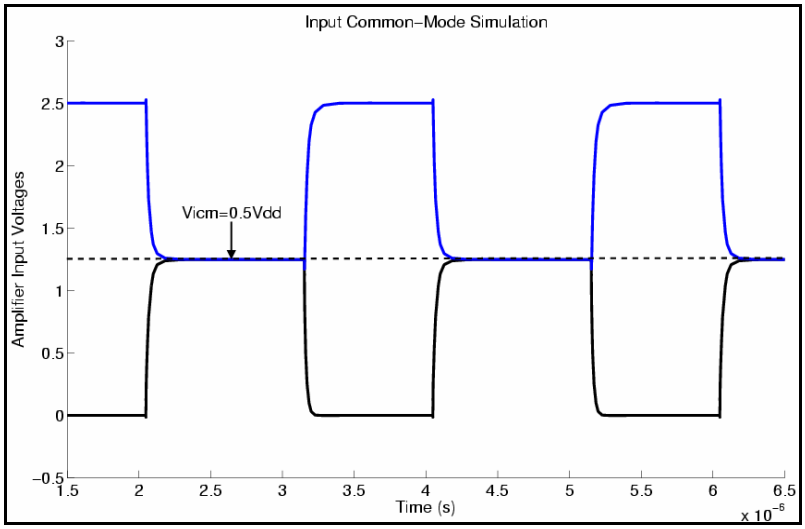



Figure 3.27: Input simulation results of the reference-capacitor-less SC amplifier.

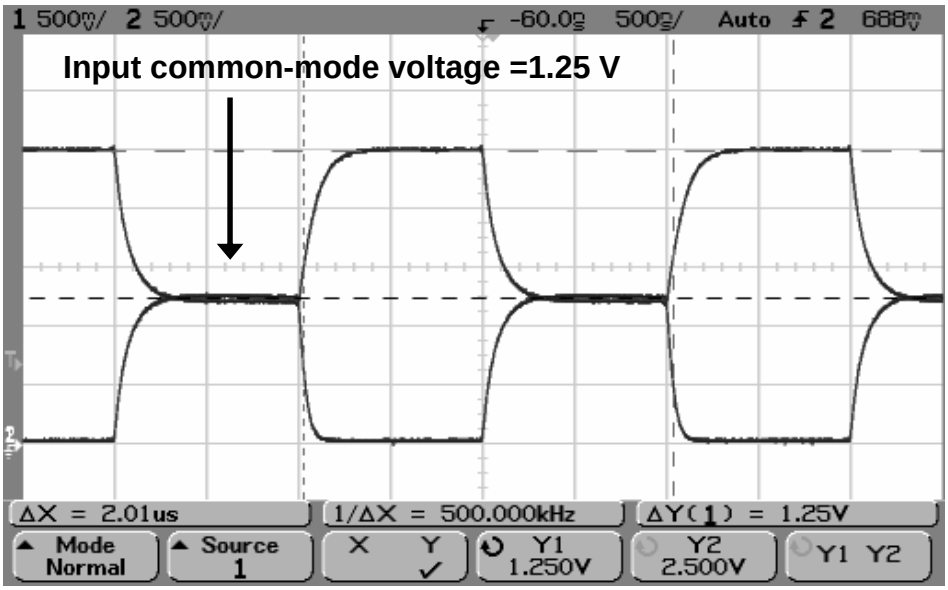



Figure 3.28: Measured input voltages of the new SC charge amplifier ($V_{ICM}=0.5V_{DD}$ )

Measured specifications are in good agreement with the simulation results. The fabricated micro-gravity SOI accelerometer was interfaced to the IC through wirebonds and was tested under the static and dynamic accelerations. Figure 3.29 shows the picture of a custom-designed PCB to measure the performance of the accelerometer-IC system.

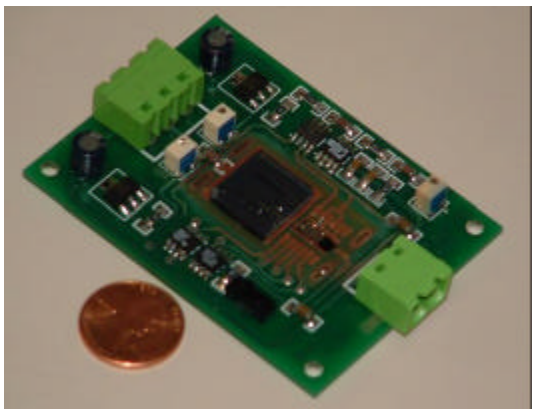


Figure 3.29: Custom-designed PCB to test the micro-gravity accelerometer-IC.

A low power consumption of 6 mW (with a sampling clock of 500 kHz) has been achieved. Figure 3.30 shows the static response of the accelerometer to the five-point acceleration test (0g, ±0.5g and ±1g applied using a dividing head, a rotary disk with

fine divisions to apply fractions of gravity to an accelerometer attached to it). It has a measured linear gain of 1 V/g, corresponding to a capacitive sensitivity of 1 pF/g. Three snap shots of the accelerometer response to +1g, 0g and –1g are provided in Figure 3.31.

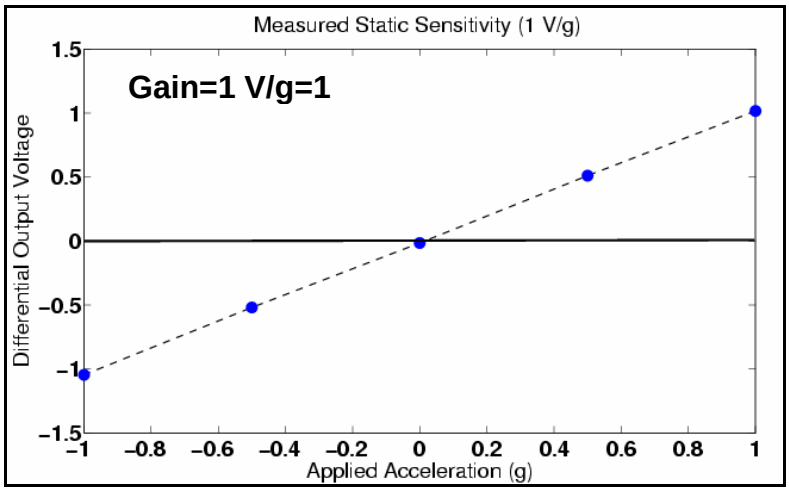



Figure 3.30: Static test result showing the output voltage of the IC chip vs. acceleration in the range of ±1g.

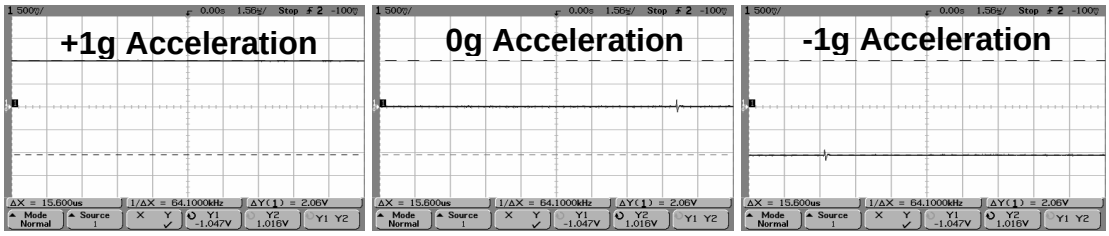



Figure 3.31: Static output variation for three different DC accelerations.

Figure 3.32 shows the dynamic response of the accelerometer mounted on top of a horizontal shaker table to a 2 Hz, 0.7g peak acceleration (the interface IC is configured for a gain of 1 V/g). The horizontal shaker table helps to avoid gravitational acceleration and therefore it was possible to have the sinusoidal response around zero acceleration. The accelerometer was calibrated through its own static response that was measured before.

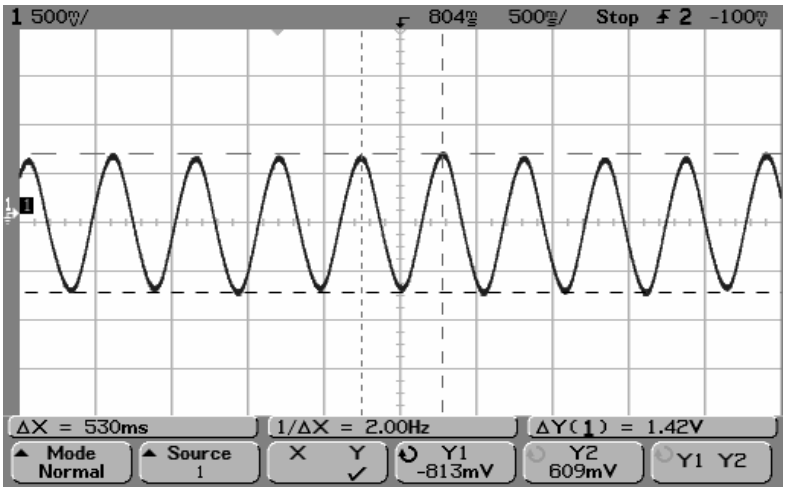



Figure 3.32: Time domain response to an input acceleration of 0.7g (peak) at 2 Hz.

The MEMS-IC measured noise spectrum is shown in Figure 3.33. The corresponding acceleration resolution for the measured noise of -95 dBm/Hz at 2.5 Hz (RBW=1 Hz) is equal to 6 μg/√Hz. The corresponding capacitive resolution is 6 aF/√Hz (at 2.5 Hz).

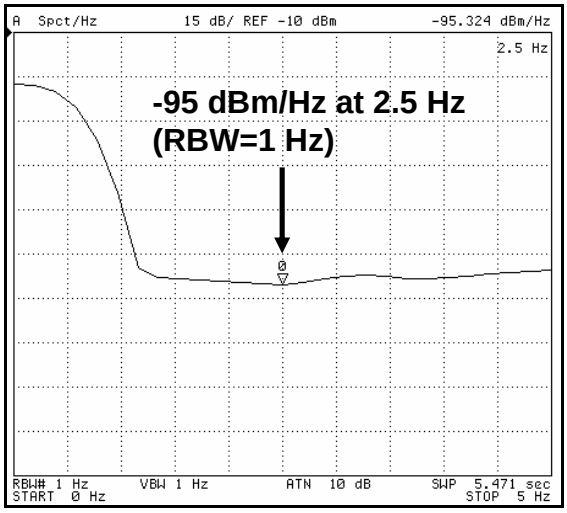



Figure 3.33: Output noise power spectrum of accelerometer system.

Table 3.2 summarizes the measured characteristics of the micro-gravity SOI accelerometer with the readout interface IC.

Table 3.2: Measured specifications of the micro-gravity SOI accelerometer-IC chip.

| **Accelerometer** | |
|---|---|
| Proof mass size | 2 mm × 6 mm |
| Overall sensor size | 5 mm × 6 mm |
| Device thickness | 50 μm |
| Capacitive gap size | 2.3 μm |
| Mass *(M)* | 1.6 milli-gram |
| Rest capacitance *($C_S$)* | 9 pF |
| Static sensitivity | 0.8 pF/g |
| *BNEA* | <1 μg/√Hz |
| Sensor bandwidth | 1.6 kHz |
| **Interface IC with the MEMS** | |
| Power supply | GND-2.5 V |
| Output noise floor | -95 dBm @2.5 Hz (*RBW*=1 Hz) |
| *TNEA* | 6 μg @2.5 Hz (*RBW*=1 Hz) |
| Capacitance resolution | 6 aF @2.5 Hz (*RBW*=1 Hz) |
| Gain | 1 V/g |
| Max. output swing | 2 V |
| Max. input acceleration | 2g |
| Dynamic range | 110 dB @ 2.5 Hz |
| Sampling clock | 500 kHz |
| Power dissipation | 6 mW |
| Active die area | 0.2 $mm^2$ |

## 3.6 SUMMARY

The design and implementation of a generic SC charge amplifier with a new input switching scheme was presented for capacitive readout of the SOI accelerometers. This architecture eliminated the need for area-consuming on-chip reference capacitors and provided more versatility over the sensor selection. A micro-gravity SOI accelerometer (introduced in Section 2.3) was interfaced with amplifier and characteristic specifications were obtained. Test results indicated that discrete-time signal processing was still one of the best candidates for high precision instrumentation systems. The interface IC was fabricated in a 0.25 μm CMOS process operating from a single 2.5V supply and wire-bonded to the accelerometer chip. A low power consumption of 6 mW with a sampling clock of 500 kHz was measured. The effective die area was 0.2 $mm^2$ including programmable amplification capacitors. It demonstrated over 75% die size reduction compared to a previously reported accelerometer interface circuit [74]. In order to reduce the circuit noise equivalent acceleration (*CNEA)* and improve the dynamic range, low frequency noise and offset reduction techniques, i.e., correlated double sampling (CDS) scheme and optimized transistor sizing were deployed. Moreover, the fully-differential input-output scheme helped to reduce the background common mode noise signals. The measured resolution of the accelerometer system was 6 μg/√Hz with an output dynamic range of 110 dB at 2.5 Hz.

# CHAPTER 4

# ANALOG-OUTPUT SUB-MICRO-GRAVITY SOI ACCELEROMETER

## 4.1 OVERVIEW

In section 2.4, an added-mass capacitive SOI accelerometer with sub-micro-gravity resolution and high sensitivity (in the order of 50 pF/g) was designed and implemented. The very low-bandwidth (<10 Hz) requirement of sub-micro-gravity accelerometers necessitates significant low-frequency noise reduction and band limiting, which are achieved through the use of the CDS scheme in a reference-capacitor-less SC charge amplifier followed by an SC low-pass filter (SC LPF). Also, the accelerometer should provide a high capacitive sensitivity to improve the noise performance, which translates into a larger rest capacitance and larger time constants.

In this chapter, the design and implementation of a readout/band-limiting IC is presented to interface with the solid proof mass sub-micro-gravity SOI accelerometer. The interface IC is implemented in the 3 V 0.5 μm 2P3M N-well CMOS process from AMI Semiconductor (AMIS) and is wirebonded to the accelerometer die. The entire system is tested for static, dynamic and noise characteristics, and measured performance data is provided.

## 4.2 CMOS INTERFACE CIRCUIT ARCHITECTURE

The proposed sub-micro-gravity SOI accelerometer and IC should have a very small bandwidth (<10 Hz). The sensor's mechanical response can not provide a $BW_{-3dB}$ of less than 100 Hz even with increased proof mass and reduced stiffness. Therefore, the output bandwidth of the accelerometer should be limited by the support electronics. For this purpose, a programmable-gain reference-capacitor-less SC charge amplifier (front-end block) and a first-order SC low-pass filter (SC LPF) followed by an instrumentation amplifier (back-end block) are designed. The circuit low-frequency noise is improved by using the CDS capacitors in the front-end block. The instrumentation amplifier converts the differential output to a single-ended output voltage that can be further band-limited through an external *RC* filter. Figure 4.1 shows the schematic diagram of the proposed interface IC.

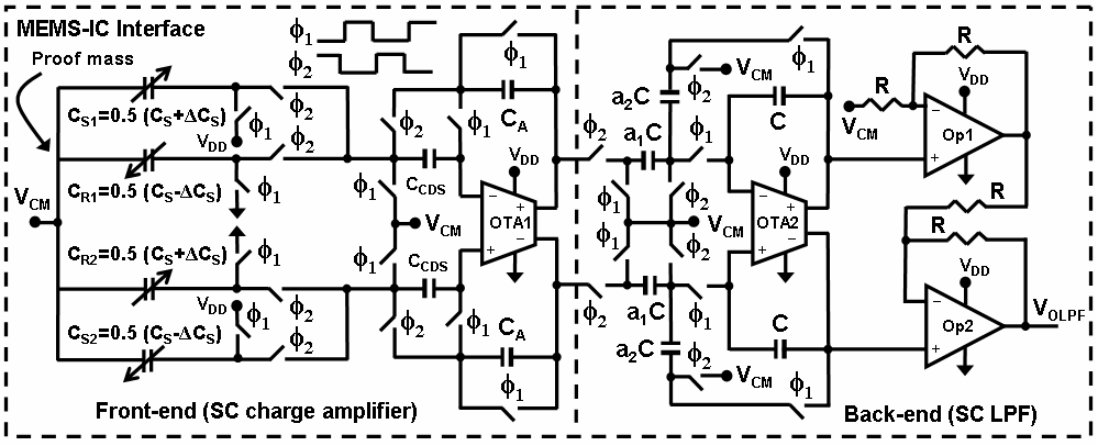



Figure 4.1: Schematic diagram of the interface IC for the sub-micro-gravity SOI accelerometer.

In the following sections, the design and implementation of the OTA, SC LPF and the instrumentation amplifier is discussed in detail. Each block is simulated and tested for proper functionality. The interface circuit is implemented in the 3 V 0.5 µm 2P3M N-well CMOS process from AMI Semiconductor (AMIS), supported through MOSIS.

## 4.3 DIFFERENTIAL FOLDED-REGULATED-CASCODE OTA

In chapter 3, a regular fully-differential folded-cascode OTA was introduced. The limited gain of the OTA caused the CDS scheme to degrade when the sense capacitance of the microaccelerometer was large. For sub-micro-gravity capacitive SOI accelerometers, the rest capacitance is even larger that puts limitations on the CDS efficiency. Therefore, a gain boosting technique was developed to increase the gain of the amplifier. The idea behind this technique is to further increase the output impedance without adding more cascode devices [81]. In this section, the design and implementation of a low-power high-performance folded-regulated-cascode OTA is described. Table 4.1 shows the required specifications of the OTA that is the core op amp in front-end and back-end blocks.

Table 4.1: Projected specifications of the core OTA.

| | |
|---|---|
| Single power supply *($V_{DD}$)* | 3 V |
| Total current budget | 200 µA |
| Max. diff. output swing | $2(V_{DD}-1)$ V |
| Open-loop gain *($A_{V0}$)* | >80 dB |
| Unity gain bandwidth *(GBW)* | >3 MHz |
| Phase margin *(PM)* | >60° *($C_{LOAD}$=2 pF)* |
| Output common mode *($V_{OCM}$)* | $0.5V_{DD}$ |
| Slew rate *(SR)* | 10 V/µs |
| Common mode rejection ratio *(CMRR)* | >60dB |

Figure 4.2 demonstrates the schematic diagram of the proposed OTA. Four error amplifiers *(A1, A2, A3 & A4)* are used to increase the OTA output resistance by the open-loop gain. Also, they keep the active load pairs *(M3,4 & M9,10)* close to the edge of the ohmic-saturation region with the equal drain-source voltages that maximizes the output differential swing and keeps their biasing currents the same.

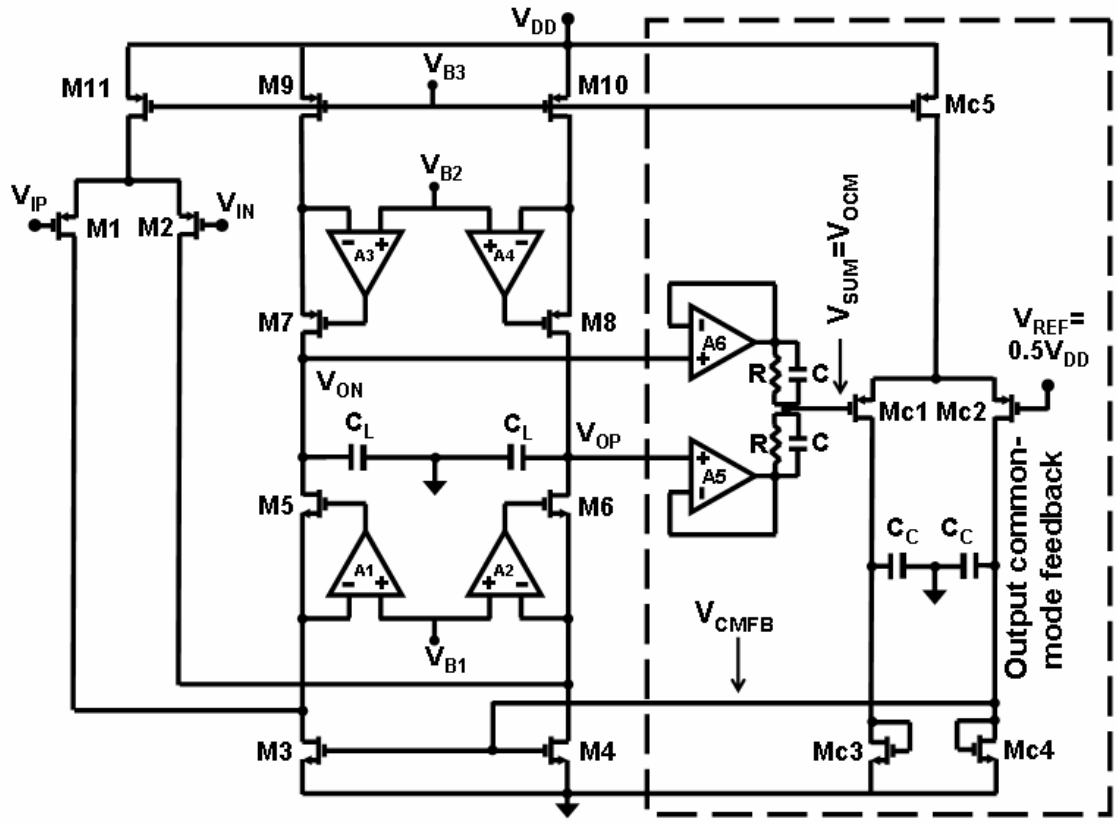



Figure 4.2: Schematic diagram of a gain boosted folded-cascode OTA.

The output common mode feedback consists of two buffer amplifiers *(A6, A7)*, a resistive summing network and a simple differential amplifier *(Mc1, Mc2)*. The output common-mode voltage is sensed resistively and compared with a reference voltage *($V_{REF}$)* through the simple differential amplifier. Then, a common-mode feedback voltage *($V_{CMFB}$)* is generated to control the biasing voltage of the load transistors *(M3, M4)*. The imposed negative feedback loop keeps the output common-mode voltage *($V_{OCM}$)* at the half of the rail. The stability of the loop is provided by the use of compensation capacitors *(C, $C_C$)* and it is tested for instability problems.

### 4.3.1 AMPLIFIER-AUGMENTED CURRENT SOURCE

Providing a main current source (to bias different transistors in the amplifier) is an important step in the analog IC design. The main current source should remain constant with respect to the power supply and temperature variations. In the following section, an amplifier-augmented bootstrapped current source is introduced (Figure 4.3). The design specifications are summarized in Table 4.2.

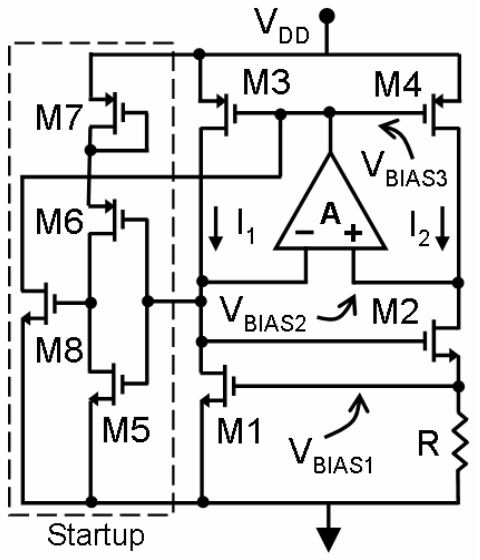



Figure 4.3: Schematic diagram of a wide supply $V_T$-current source and startup circuit.

Table 4.2: Bias specifications of the main current source.

| | |
|---|---|
| Supply voltage | 2.5-3.3 V |
| Main current source | 10 µA |
| $V_{BIAS1}$ | 0.9 V |
| $V_{BIAS2}$ | 2 V |
| $V_{BIAS3}$ | Supply-ratiometric |
| Supply sensitivity | <15 ppm/V |

The error amplifier is used to set $V_{SD4}$ equal to $V_{SD3}$. Therefore, transistors *M3* and *M4* show the same channel length modulation effect and their currents are exactly equal. In addition, they are biased close to the edge of the ohmic-saturation region to reduce

the minimum operating voltage to 2.5 V that guarantees the proper operation with 3 V supply. At the startup, *M8* forces a non-zero current through *M2* and *R* to build up the gate-source biasing of the transistor *M1* and to establish the equilibrium bias point of $I_1=I_2=10\ \mu A$ *(R=90 kW).* In this design, the gate lengths of the critical transistors are set to 3 μm to reduce the channel length modulation effect and increase the output resistance of the individual transistors. The error amplifier is a single stage differential amplifier that sets the DC values of the biasing points correctly (Figure 4.4).

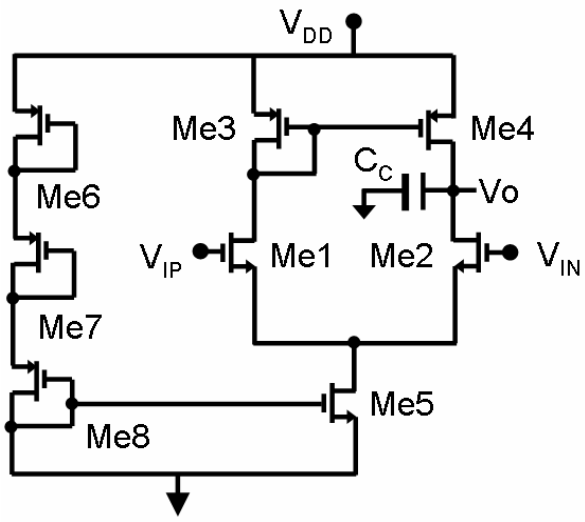



Figure 4.4: Schematic diagram of an error amplifier.

The simulation results confirm that the designed current source operates properly with a power supply in the range of 2.5 to 3.3 V and shows less than 15 ppm/V voltage dependency to the supply (Figure 4.5). However, the temperature coefficient (TC) of the current reference depends on the TC of the resistor *R* that is measured to be about 300 ppm/°C. Figure 4.6 shows the I-V characteristic of the current source when the supply is swept from 0 to 3.5 V. The stable point of $I_1=I_2=10\ \mu A$ is realized. The designed current source is used to bias the fully-differential folded-regulated-cascode OTA.

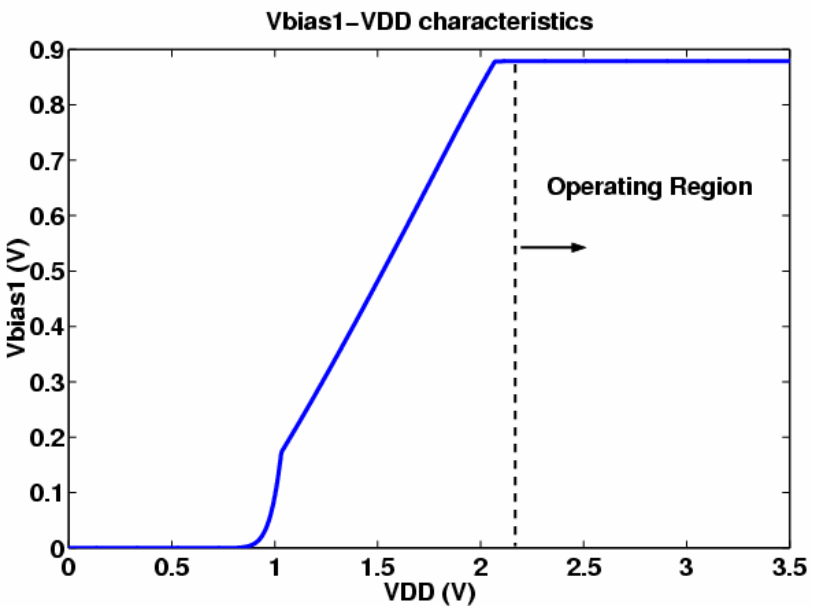



Figure 4.5: $V_{BIAS1}$ versus supply changes.

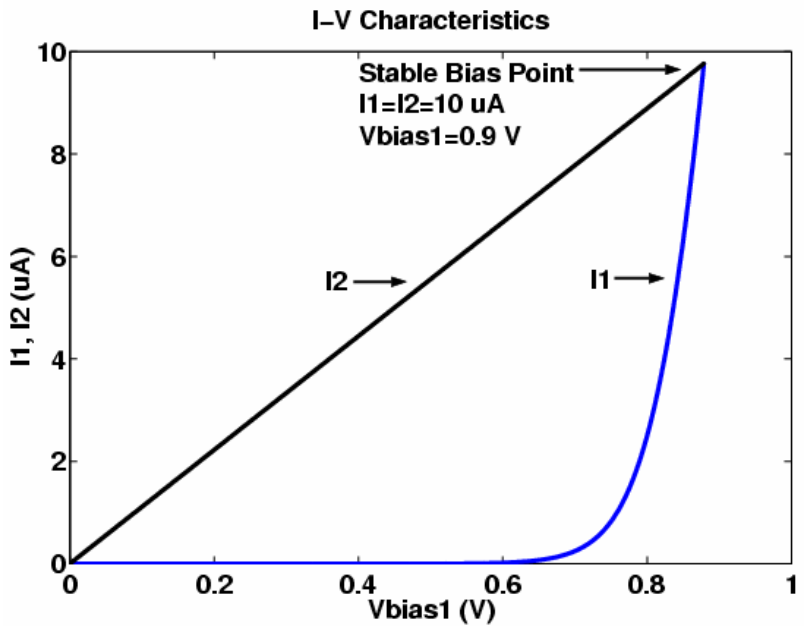
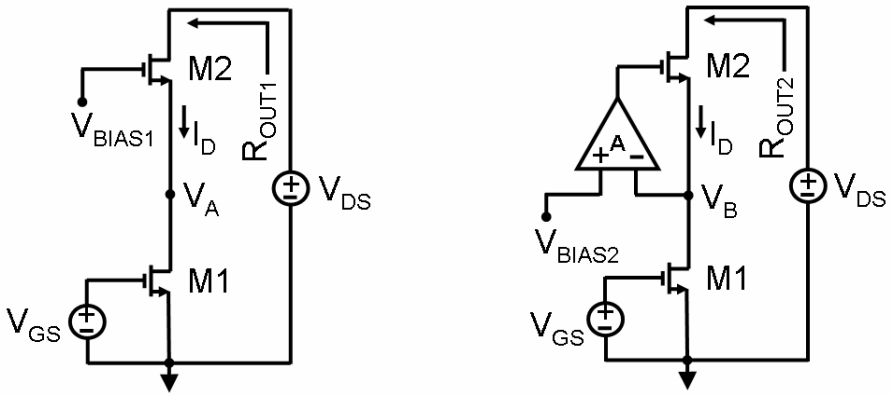



Figure 4.6: *I-V* characteristics for the equilibrium biasing point.

### 4.3.2 REGULATED-CASCODE AMPLIFIER

Figure 4.7 shows a simple cascode amplifier and an improved cascode amplifier that are arranged for the output resistance simulation.




(a) (b)

Figure 4.7: (a) A simple cascode amplifier; (b) An active-cascode amplifier.

The output resistance of the simple cascode amplifier is equal to

$$R_{OUT1} = g_{m2} r_{O1} r_{O2} \tag{4-1}$$

In Figure 4.7.a, *M1* operates as a degeneration resistor that senses the output current and converts it to a voltage at the output of *M2*. It acts as a series-series feedback that increases the output impedance. In a boosted-cascode amplifier (Figure 4.7.b), the idea is to drive the gate of *M2* by an amplifier *(A)* that forces $V_B$ to be equal to $V_{BIAS2}$. Thus, voltage variations at the drain of *M2* now affect $V_B$ to a smaller extent (compared to $V_A$) because the amplifier *A* regulates this voltage. With smaller variations at $V_B$, the current through *M1* and hence the output current remain more constant. The output resistance of the active-cascode amplifier is boosted by the gain of the amplifier and is equal to

$$R_{OUT2} = A g_{m2} r_{O1} r_{O2} \tag{4-2}$$

The $I_{OUT}$-$V_{OUT}$ characteristics of a simple cascode amplifier (dashed line) and a regulated-cascode amplifier (solid line) for three different gate biasing voltages are plotted in Figure 4.8. The inverse slope of the curves represents the output resistance.

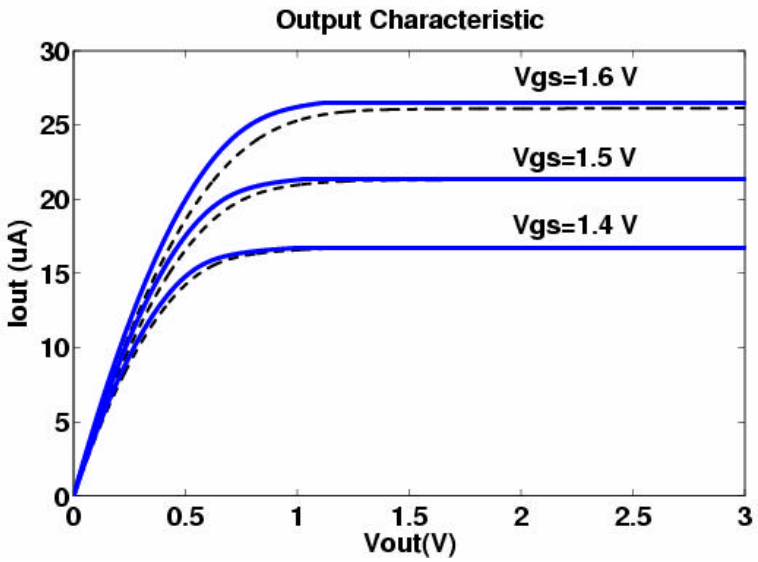



Figure 4.8: $I_{DS}$-$V_{DS}$ characteristic of a simple cascode amplifier (dashed curve) and a boosted cascode amplifier (solid curve) for different gate bias voltages.

The output resistance of the regulated-cascode amplifier shows a significant increase (88 dB) compared to the simple cascode amplifier (Table 4.3). Transistors are selected from the standard 3 V 0.5 µm CMOS process.

Table 4.3: Design specifications of the simulated circuit in Figure 4.7.

| | Simple Cascode | Regulated-Cascode |
|---|---|---|
| $(W/L)_1$ | 3 µm/3 µm | 3 µm/3 µm |
| $(W/L)_2$ | 3 µm/3 µm | 3 µm/3 µm |
| $V_{GS}$ | 1.5 V | 1.5 V |
| $V_{DS}$ | 1.5 | 1.5 |
| $I_{DS}$ | 21.3 µA | 21.4 µA |
| $V_{BIAS}$ | 2.5 V | 0.8 V |
| $R_{OUT}$ | 14 MΩ | 370 GΩ |

### 4.3.3 OTA DESIGN AND SIMULATION

Design specifications of the gain boosted folded-cascode OTA (Figure 4.2) are summarized in Table 4.4.

Table 4.4: Design specifications of the OTA.

| | |
|---|---|
| Power supply | 3 V-GND |
| Current consumption | 150 μA |
| Open-loop DC gain *($A_{V0}$)* | 133 dB |
| Unity gain bandwidth *(GBW)* | 4.4 MHZ *($C_L$=2.5 pF)* |
| Phase margin *(PM)* | 72° *($C_L$=2.5 pF)* |
| Input common-mode rejection ratio *(ICMRR)* | 50 dB |
| Input common-mode voltage range *($V_{ICR}$)* | 0 to 2 V |
| Outputcommon-mode voltage *($V_{OCM}$)* | 1.5 |
| Max. differential output swing | 4 V |
| Input referred noise | 10 μV *(f=0.1 to 100 Hz)* |

The very large DC gain of the amplifier helps to improve the noise performance of the interface circuit. Moreover, common-mode noises and environmental interferences are rejected through the fully-differential scheme. Table 4.5 demonstrates the size of each transistor in the OTA circuit with a channel length of 3 μm.

Table 4.5: *W/L* ratios of the transistors in the OTA.

| Transistor | W/L ratio | Transistor | W/L ratio |
|---|---|---|---|
| *M1,2* | 110 | *Mc1,2* | 22 |
| *M3,4* | 33 | *Mc3,4* | 11 |
| *M5,6* | 22 | *Mc5* | 22 |
| *M7,8* | 22 | | |
| *M9,10* | 22 | | |
| *M11* | 22 | | |

The simulated frequency response of the OTA with a capacitive load of 2.5 pF is provided in Figure 4.9.

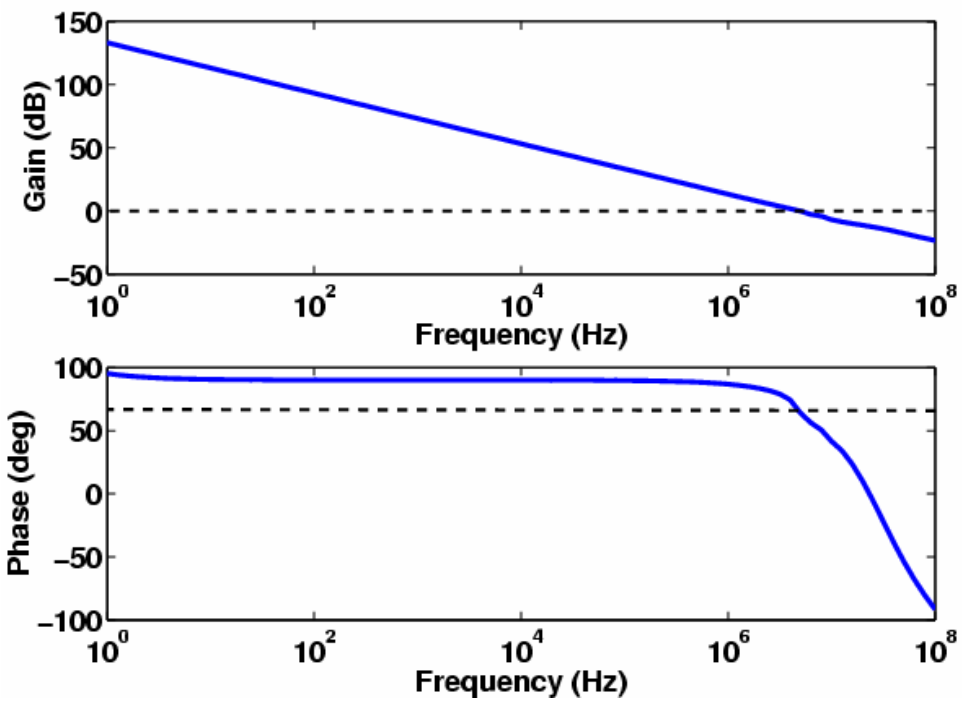



Figure 4.9: The simulated Frequency response of the differential folded-regulated-cascode OTA.

The OTA has a simulated open-loop gain of 133 dB and a *GBW* of 4.4 MHz with a *PM* of 72° for $C_L$*= 2.5 pF*. Simulated noise of the OTA in a unity gain configuration is shown in Figure 4.10. The input referred noise is 10 μV (bandwidth of 0.1 to 100).

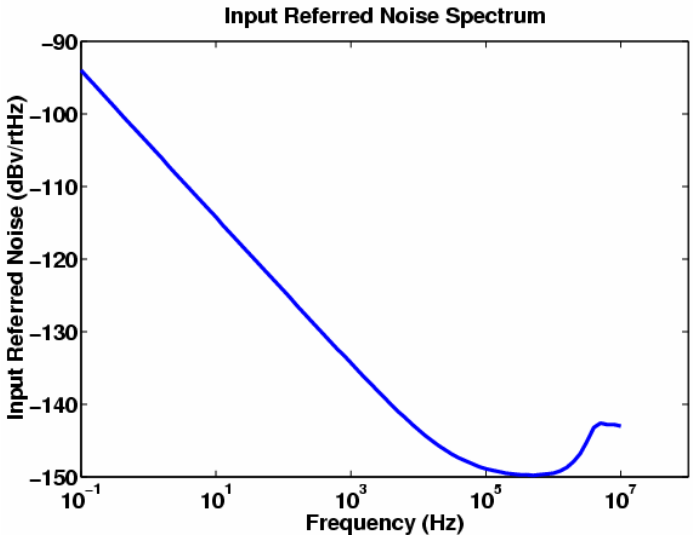



Figure 4.10: Simulated output noise spectrum of the OTA.

A switched-capacitor voltage amplifier was designed to test the OTA performance. Figure 4.11 shows the schematic diagram of the programmable SC voltage amplifier. A CDS capacitance of 5 pF was used in this design.

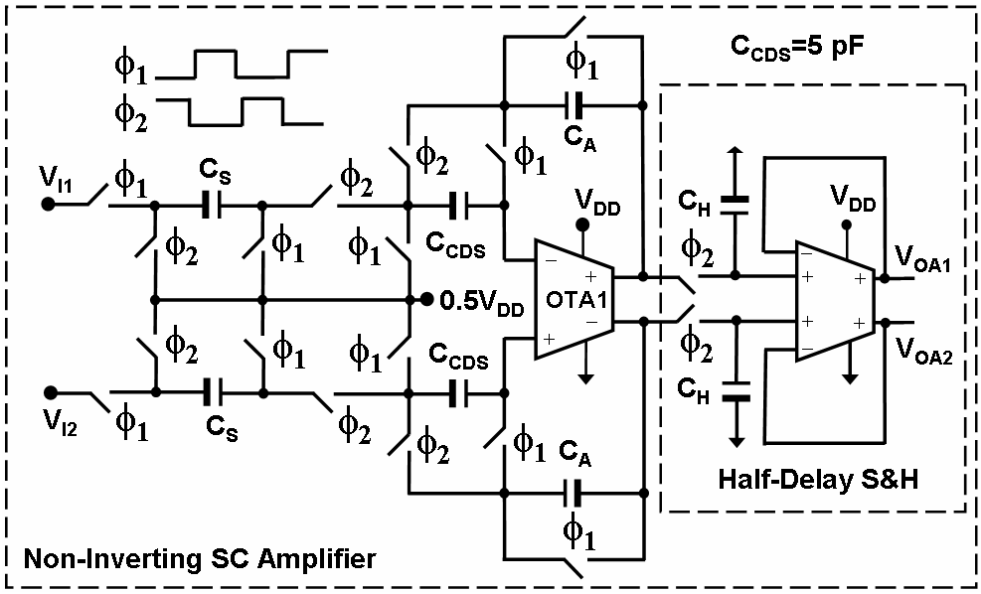
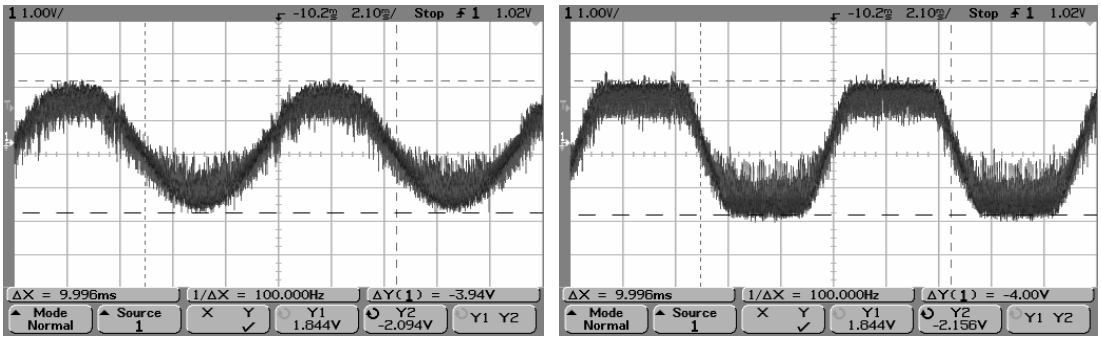



Figure 4.11: Schematic diagram of a non-inverting SC amplifier.

The measured differential output swing of the amplifier is 4 V with a supply of 3 V (Figure 4.12).




(a) (b)

Figure 4.12: (a) Maximum output swing; (b) Over-driven output swing.

The chip microphotograph is shown in Figure 4.13. The core IC size is 0.4 $mm^2$ and it measures a power consumption of 1.5 mW with a sampling clock of 40 kHz.

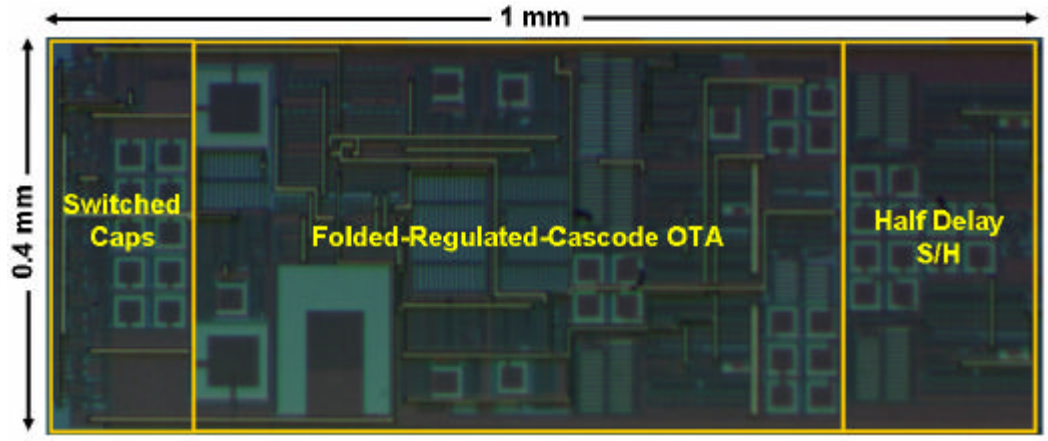



Figure 4.13: Chip microphotograph of the non-inverting SC amplifier

## 4.4 SWITCHED CAPACITOR LOW-PASS FILTER

A first-order low-pass filter is the most basic filter that is determined by two parameters: DC gain and -3 dB frequency. SC integrators are extensively used to implement discrete-time integrated filters [15]. The schematic diagram of a first-order SC LPF and an instrumentation amplifier, designed in the back-end block, are shown in Figure 4.14.

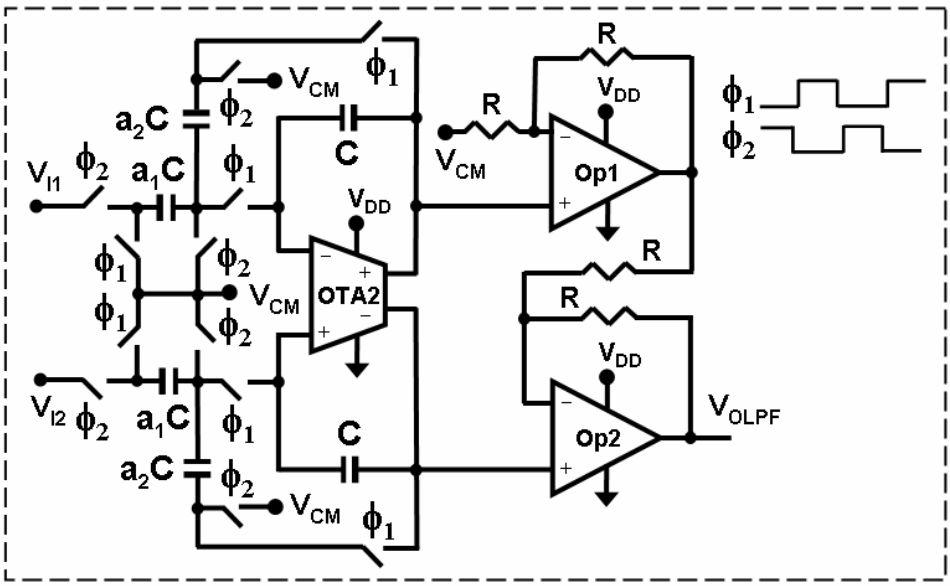



Figure 4.14: Circuit diagram of a first-order SC LPF and instrumentation amplifier.

The *S*-domain transfer function of the filter is equal to [15] [83]

$$H(s) = \frac{a_1 / a_2}{1 + \frac{s}{a_1 f_S}} = \frac{T_0}{1 + \frac{s}{w_{-3dB}}} \tag{3-3}$$

where $f_S$ is the sampling clock, $a_1$ is the ratio of the forward capacitance to the integration capacitance, and $a_2$ is the coefficient of the feedback capacitance to the integration capacitance. The filter is designed for a unity DC gain $(T_0=1)$ and it has a programmable -3dB bandwidth that is set by the clock frequency. For example, for a filter $BW_{-3dB}$ of 200 Hz (equal to the sensor $BW_{-3dB}$), we have

$$T_0 = 1, w_{-3dB} = 400p\,,\ f_S = 40kHz \Rightarrow a = a_1 = a_2 = \frac{w_{-3dB}}{f_S} = 0.031416 \tag{3-4}$$

In this implementation, the total capacitance is

$$C_T = 2\left(C_U + \frac{C_U}{a_1} + \frac{C_U}{a_2}\right) = 2\left(1 + \frac{2}{a}\right)C_U \tag{3-5}$$

For a unit capacitance $(C_U)$ of 100 fF, the total capacitance is 13 pF, which is possible to fabricate on-chip. The integrator capacitor *(C)* is large enough to act as a sample and hold at the output of the filter. The instrumentation amplifier provides an extra gain of 2 and changes the output to a single-ended signal. An external *RC* filter is used for additional band-limiting of the output signal.

## 4.5 SUB-MICRO-GRAVITY SENSOR-IC TEST RESULTS

Figure 4.15 shows the chip microphotograph that was wire-bonded to the sub-micro-gravity accelerometer on a test board.

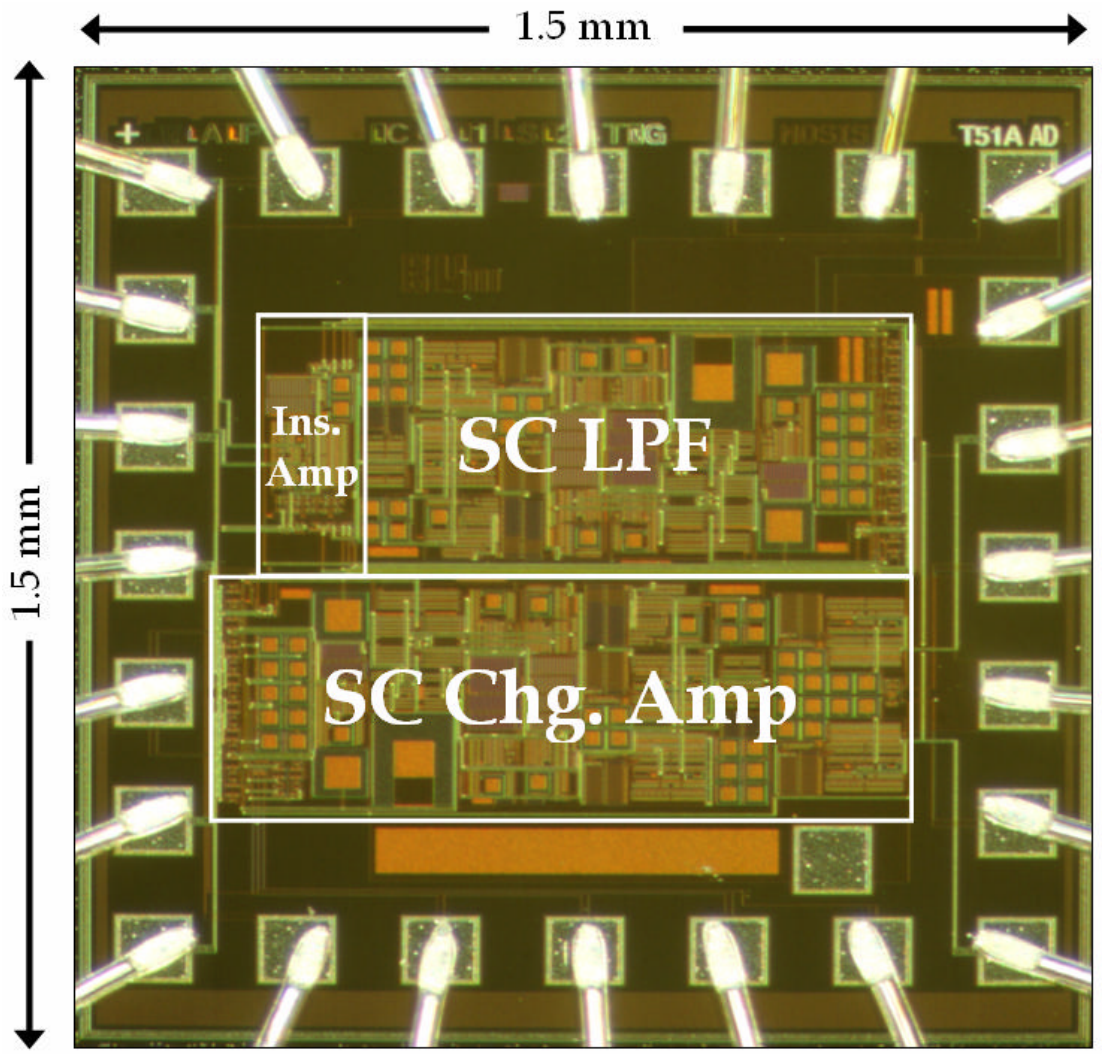



Figure 4.15: Chip microphotograph (Chip area: 2.25 $mm^2$).

A low power consumption of 4 mW has been achieved with a sampling clock of 40 kHz. The IC chip measures an area of 2.25 $mm^2$. The static response of the accelerometer is provided in Figure 4.16. The IC output saturates with less than 20 mg (<2° tilt from earth surface). The measured voltage gain $(V_O/g)$ is 105 mV/mg.

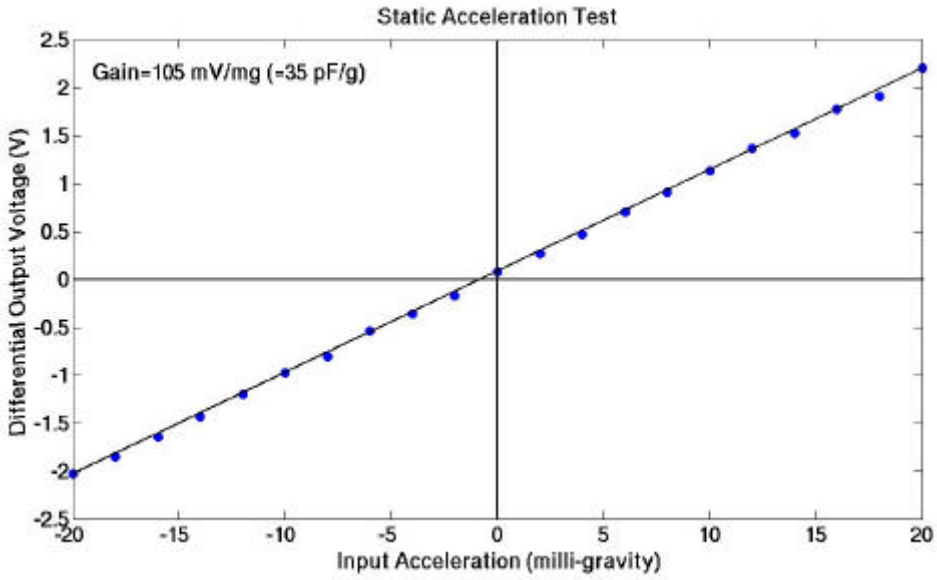
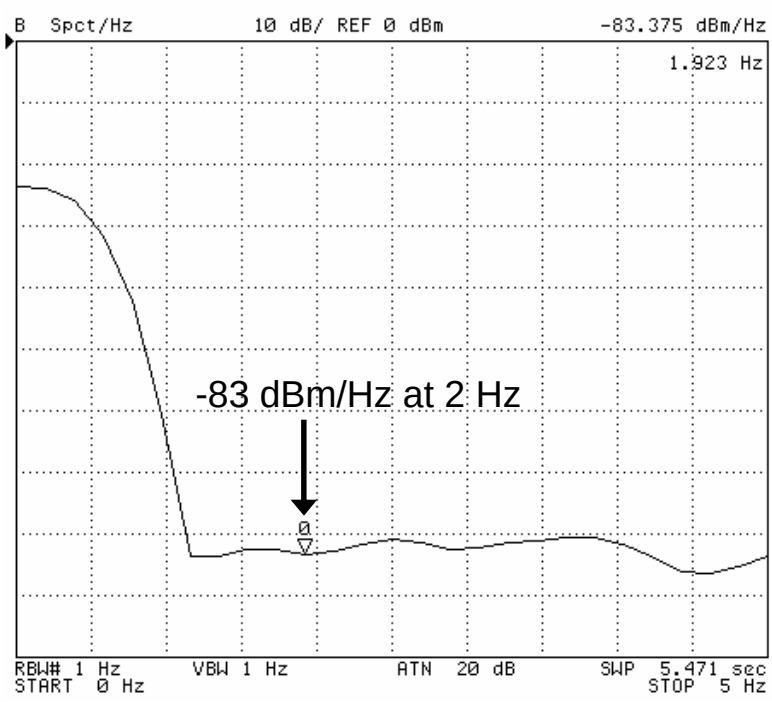
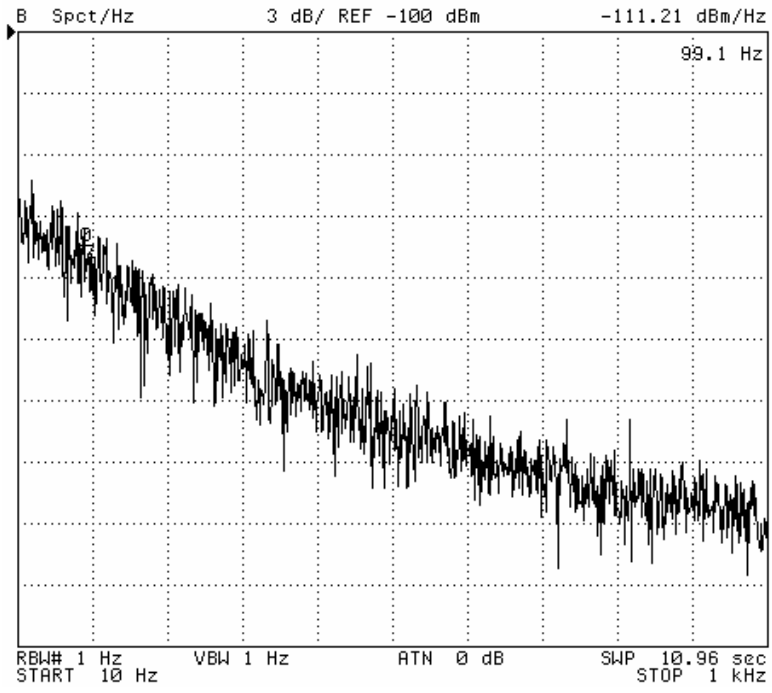



Figure 4.16: Static response of the accelerometer within ±20 milli-g.

The measured output noise floor of the MEMS-IC chip is -83 dBm/Hz at 2 Hz (corresponding to an acceleration resolution of 213 ng/√Hz) (Figure 4.17). The SC LPF is set for the maximum $BW_{-3dB}$ of 200 Hz, equal to the sensor bandwidth. In addition, an external *RC* low-pass filter is used at the output of the instrumentation amplifier, to band-limit the output signal to 5 Hz. It was observed that the operation of the SC LPF was degraded for the smaller sampling clocks (<40 kHz), mainly due to the leakage of the CMOS switches and small hold capacitances. Therefore, it was not possible to push the filter's bandwidth below 200 Hz and an external RC filter was added to limit the filter's bandwidth. A future solution to this problem is the design of very small length CMOS switches with charge pump sampling clocks. In addition, the increase of the unit capacitance is helpful if more chip area is accessible.




(a)




(b)

Figure 4.17: (a) MEMS-IC low-frequency noise measurement; (b) IC flicker noise profile.

The dynamic response of the accelerometer to an external acceleration of 16 mg (peak) at 230 mHz is shown in Figure 4.18. CH1 shows the differential output of the

interface IC without external low-pass filter. Due to extremely high sensitivity of the accelerometer, the device picks up any external vibration of the test setup (and hence the noisy response of the CH1). CH2 shows the differential output after an external *RC* filter with $BW_{-3dB}$ of 5 Hz. The signal is effectively cleaned. The measured specifications are summarized in Table 4.6.

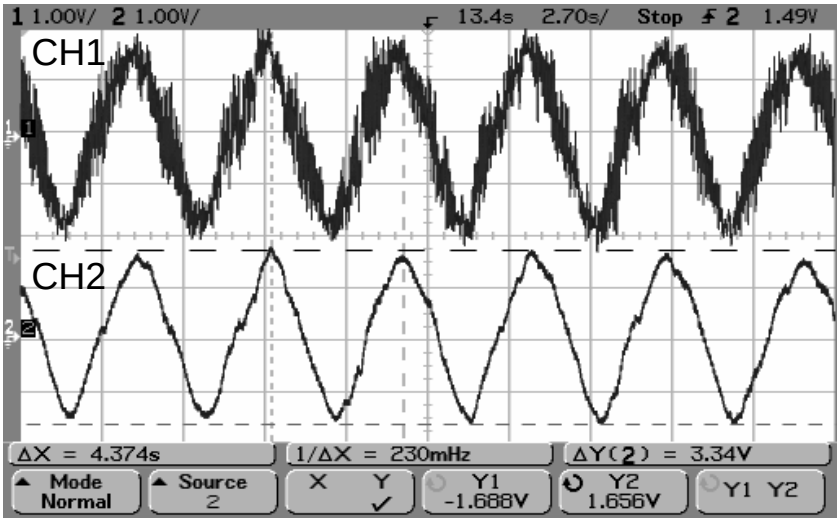



Figure 4.18: MEMS-IC output response to an acceleration of 16 mg (peak) 0.23 Hz.

Table 4.6: Measured specifications of sub-micro-gravity SOI accelerometer-IC chip.

| **Accelerometer** | |
|---|---|
| Dimensions:<br>Top-side proof mass<br>Extra seismic mass | <br>7 mm × 5 mm × 100 μm<br>6.7 mm × 4.7 mm × 400 μm |
| Proof mass | 38 milli-gram |
| Reduced gap size | 5 μm |
| Sensitivity | 35 pF/g |
| Brownian noise floor | 50 nano-g/√Hz |
| $f_{-3dB}$ (1st-flexural) | 200 Hz |
| 2nd-mode (out-of-plane) | 1300 Hz |
| **Interface IC with the MEMS** | |
| Power supply | GND-3 V |
| Filter $BW_{-3dB}$ | 5 Hz (external *RC*) |
| Output noise floor | -83 dBm @2 Hz (*RBW*=1 Hz) |
| *TNEA* | 213 nano-g @2 Hz |
| Capacitive resolution | 7 aF @2 Hz |
| Gain | 105 mV/milli-g |
| Max. linear output swing | 3 V |
| Max. input acceleration | 30 milli-g |
| Dynamic range | 103 dB |
| Power dissipation | 4 mW |
| Sampling frequency | 40 kHz |
| Die overall area | 2.25 $mm^2$ |

## 4.6 SUMMARY

The implementation and characterization of a novel in-plane capacitive microaccelerometer-IC with sub-micro-gravity resolution and high sensitivity was presented. As described in Section 2.4, the accelerometer fabrication process flow was stictionless and very simple compared to some other microaccelerometer fabrication technologies that used regular silicon substrates with multi-mask sets [42] [84]. The accelerometer was wirebonded to an SC interface circuit. The interface IC was based on a front-end SC charge amplifier and a back-end SC LPF with an instrumentation amplifier and was implemented in the standard 3 V 0.5 μm CMOS process. The measured capacitive sensitivity *($DC_S$/gravity)* was 35 pF/g and the overall gain of the system was 105 mV/mg. The IC measures power consumption of 4 mW with a sampling clock of 40 kHz. The die size was 2.25 $mm^2$. Based on the measured data, this accelerometer system is one of the most sensitive MEMS accelerometers that have been presented so far.

# CHAPTER 5

# OPEN-LOOP SD CMOS-SOI ACCELEROMETER

## 5.1 OVERVIEW

The demand of powerful digital signal processors implemented in CMOS technologies (optimized for digital circuits) raises the need for robust high-resolution analog-to-digital (A/D) and digital-to-analog (D/A) converters. Converters should be integrated on the same substrate with the digital circuitry and provide high performance functionality. Oversampling A/D and D/A converters or so-called Sigma-Delta (ΣΔ) modulators are the most suitable converters for low-frequency high-resolution applications that can provide this requirement. ΣΔ modulators are based on trading off accuracy in amplitude for accuracy in time to avoid the difficulty of implementing complex precision analog circuits [85] [86]. Nowadays, low-cost and small footprint digital MEMS accelerometers with high sensitivity, high resolution, and low power consumption are required in a vast number of applications ranging from portable apparatus to guidance and stabilization of satellites and spacecrafts.

In this chapter, a 2.5 V 0.25 μm CMOS first-order ΣΔ modulator for the open-loop readout of the capacitive SOI accelerometers is presented. The interface IC is based on a front-end programmable SC charge amplifier and a back-end first-order SC ΣΔ modulator. This architecture decouples the MEMS sensor from the optimized-performance ΣΔ modulator. The accelerometer is designed and implemented in 40 μm thick SOI wafer through the same process described in Section 2.3 and is wirebonded to the IC chip. The measured characteristics are provided for static and dynamic tests.

## 5.2 OPERATION OF A SD MODULATOR

Figure 5.1 depicts a first-order ΣΔ modulator that consists of an integrator, a coarse quantizer (usually 2-level quantizer) and a feedback loop that employs filters. This simple modulator is examined to explain the operation of the ΣΔ converters.

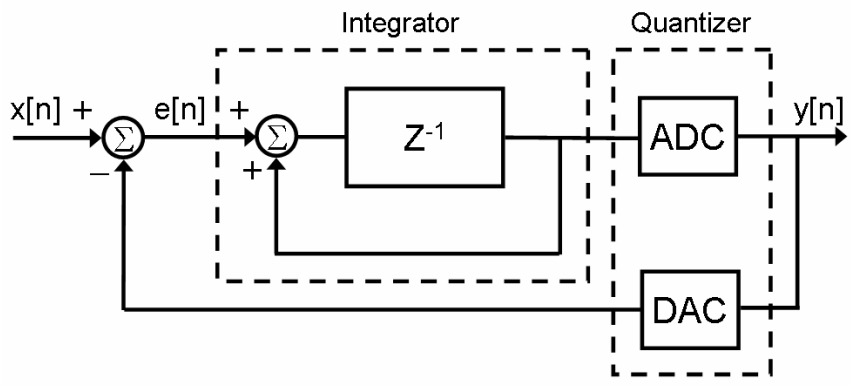



Figure 5.1 Block diagram of a first-order ΣΔ modulator.

For the case of a 2-level quantizer, the ADC and DAC of Figure 5.1 reduce to a simple clocked-comparator with a direct feedback connection. To develop a linear presentation for the modulator and characterize the spectral response of the quantization noise, the following assumptions (Bennett's criteria) are made concerning the input signal [75] [87]:

1. The modulator's input signal falls within the DAC's output levels. Hence, no saturation of the digital output code occurs. In other words, exceeding the normal operating range of the ΣΔ ADC affects the quantization noise spectrum by adding spurs (tones) or spikes to the output spectrum.

2. The modulator's least-significant-bit (LSB) is much smaller than the input signal amplitude. Otherwise, the output of the modulator can look like square wave and results in tonal output spectral. However, adding or subtracting a fed

back signal based on the expected or past quantization noise helps to avoid these spurs.

3. The input signal is busy (unpredicted) with no DC or very low-frequency components. In other words, no two consecutive outputs of the modulator have the same digital code. Sometimes, adding a high frequency dither signal or pseudo-random noise to the input helps to make the input signal randomized and suppress the tones. This high-frequency noise is eventually filtered by a digital filter or an output reconstruction filter.

With these assumptions, the operation of the modulator can be better understood from the linear quantizer model of Figure 5.2, in which the quantizer is replaced by an additive quantization error source *(q[n])*. In this model, the input signal *(x[n])* is a busy signal and the quantization error values resemble uncorrelated samples with a flat frequency spectrum.

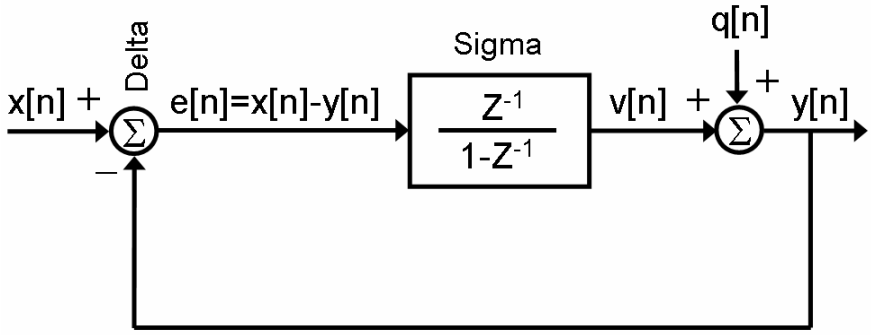



Figure 5.2: Linearized model of a first-order ΣΔ modulator.

In Figure 5.2, the summer takes the difference *(Delta)* between the input signal and the fed back signal. The integrator accumulates or sums *(Sigma)* this difference *(e[n])* and feeds the result *(v[n])* back to the summer, through the quantizer (ADC, DAC). This process forces the output of the modulator to track the average value of the input. Sometimes the fed back signal is greater than the input and other times it is smaller

than the input signal. However, the *average* fed back signal should ideally be the same as the input signal. ΣΔ modulators are oversampling converters, which means that the quantization noise power is spread over the wide sampling frequency range and only small part of it falls in the signal band. The ratio of the sampling frequency over the Nyquist rate (twice of the signal bandwidth of $f_B$) is called the oversampling ratio *(OSR).* The quantization noise in the signal band is further suppressed by the loop gain. In this feedback system, the input signal simply passes through the modulator with a delay while the quantization noise is differentiated and pushed to higher frequencies. The output is equal to

$$Y(z) = H_X(z)\,X(z) + H_Q(z)\,Q(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)Q(z) \qquad (5\text{-}1)$$

The magnitude of the quantization noise transfer function $H_Q(z)$ is found as below [83]:

$$H_Q(z)\Big|_{z=e^{j2p\frac{f}{f_s}}} = \left(1 - e^{j2p\frac{f}{f_s}}\right) = 2j\sin\left(\frac{p\,f}{f_s}\right)e^{-jp\frac{f}{f_s}} \qquad (5\text{-}2)$$

$$\left|H_Q(z)\right|_{z=e^{j2p\frac{f}{f_s}}} = 2\sin\left(\frac{p\,f}{f_s}\right) \qquad (5\text{-}3)$$

The noise generated by a scalar quantizer with two levels equally spaced by *D* is uncorrelated and has equal probability of laying any where in between *±0.5D.* The probability density function of this error is *1/D* and is sketched in Figure 5.3.

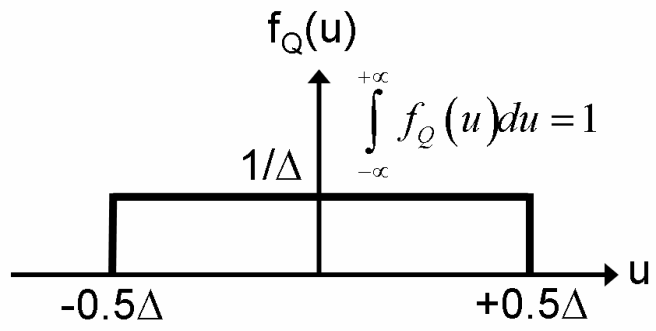



Figure 5.3: Assumed probability density function for the quantization error *q[n]*.

The average power and the power spectral density of this quantization noise are calculated as

$$P_{avg} = \left( \int_{-\infty}^{+\infty} u f(u) du \right)^2 = \left( \frac{1}{\Delta} \int_{-0.5\Delta}^{+0.5\Delta} u du \right)^2 = 0 \qquad (5\text{-}4)$$

$$S_Q^2 = \int_{-\infty}^{+\infty} u^2 f(u) du = \frac{1}{\Delta^2} \int_{-0.5\Delta}^{+0.5\Delta} u^2 du = \frac{\Delta^2}{12} \qquad (5\text{-}5)$$

The quantization noise power over the sampling frequency band of $-f_S$ to $f_S$ is equal to

$$P_Q = \int_{-f_B}^{f_B} S_Q^2(f) \left| H_Q(f) \right|^2 df = \int_{-f_B}^{f_B} \left( \frac{\Delta^2}{12} \right) \frac{1}{f_S} \left[ 2 \sin\left( \frac{p f}{f_S} \right) \right]^2 df \qquad (5\text{-}6)$$

Because of the oversampling, the signal bandwidth is much smaller than the sampling frequency (i.e. *OSR>>1*) and the following approximation is valid.

$\forall f \in f_B$ :

$$f << f_S \Rightarrow \sin\left( \frac{p f}{f_S} \right) \cong \frac{p f}{f_S}, \; P_Q \cong \left( \frac{\Delta^2}{12} \right) \left( \frac{p^2}{3} \right) \left( \frac{2 f_B}{f_S} \right)^3 = \frac{\Delta^2 p^2}{36} \left( \frac{1}{OSR} \right)^3 \qquad (5\text{-}7)$$

One can assume the input signal is a sinusoidal wave between *0* and $+V_{REF}$ and its ac power is $V_{REF}^2/8$. The best possible signal-to-noise ratio *(SNR)* for an N-bit A/D converter with quantization level of $D = V_{REF}/2^N$ and no clipping is

$$SNR_{MAX} = 10\log\left(\frac{\frac{V_{REF}^2}{8}}{\frac{V_{LSB}^2}{12}}\right) = 10\log\left(\frac{\frac{2^{2N}\Delta^2}{8}}{\frac{\Delta^2}{12}}\right) = 6.02N + 1.76dB \qquad (5\text{-}8)$$

If the same input power is used in the ΣΔ modulator, the maximum *SNR* limited by the modulator's quantization noise is

$$SNR_{MAX} = 10\log\left(\frac{P_X}{P_Q}\right) = 10\log\left(\frac{\frac{2^{2N}\Delta^2}{8}}{\left(\frac{\Delta^2}{12}\right)\left(\frac{p^2}{3}\right)\left(\frac{2f_B}{f_S}\right)^3}\right) \qquad (5\text{-}9)$$

$$\begin{aligned} SNR_{MAX} &= 6.02N + 1.76dB - 20\log\frac{p}{\sqrt{3}} + 10\log OSR^3 \\ &= 6.02N + 1.76 - 5.17 + 30\log OSR \end{aligned} \qquad (5\text{-}10)$$

This equation predicts an increase of *30logOSR* in the *SNR* of an oversampling modulator. In other words, every doubling in the *OSR* results in 1.5 bits increase in the resolution (a 9 dB increase in *SNR*). For example, with a sampling clock of 1 MHz and an input bandwidth of 1 kHz, the *OSR* is 500, which results in a remarkable increase of 81 dB in $SNR_{MAX}$ (equivalent to 13.5 bits of resolution). The overall *SNR* with a 1-bit quantizer is then equal to

$$SNR_{MAX} = 6.02 + 1.76 - 5.17 + 30\log OSR \cong 84\,dB \qquad (5\text{-}11)$$

that is equivalent to 14 bits of resolution.

The first-order ΣΔ modulator can be extended to a second-order modulator by inserting an integrator to the forward path of the modulator (Figure 5.4). The first integrator has no delay in its forward path but has one delay in its feedback loop. The second (last) integrator has one delay in its forward path but has no delay in its feedback path.

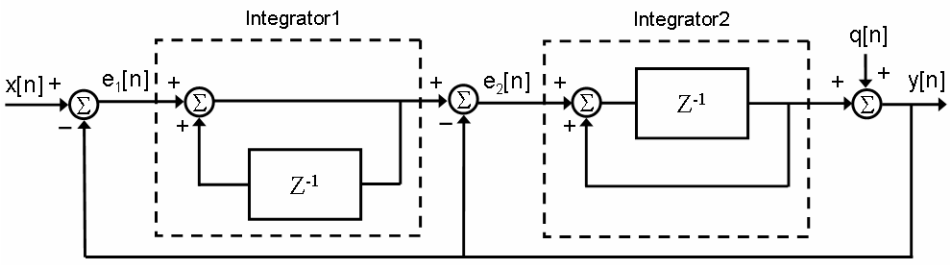



Figure 5.4: Second-order ΣΔ modulator.

The output of the second-order ΣΔ modulator in Figure 5.4 can be written as

$$Y(z) = H_X(z)\,X(z) + H_Q(z)\,Q(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)^2 Q(z) \tag{5-12}$$

The noise transfer function of $(1-z^{-1})^2$ has two zeros at DC, and provides a second-order noise shaping. In general, an *Lth*-order noise shaping can be achieved by placing $L$ integrators in the forward path of a ΣΔ modulator.

$$P_Q = \int_{-f_B}^{+f_B} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_S} \left[2\sin\left(\frac{p\,f}{f_S}\right)\right]^{2L} df \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{p^{2L}}{2L+1}\right)\left(\frac{1}{OSR}\right)^{2L+1} \tag{5-13}$$

$$SNR_{MAX} = 10\log\left(\frac{P_X}{P_Q}\right) = 10\log\left(\frac{\frac{2^{2N}\Delta^2}{8}}{\left(\frac{\Delta^2}{12}\right)\left(\frac{p^{2L}}{2L+1}\right)\left(\frac{1}{OSR}\right)^{2L+1}}\right) \tag{5-14}$$

$$\begin{aligned} SNR_{MAX} &= 6.02N + 1.76dB - 10\log\frac{p^{2L}}{2L+1} + 10\log OSR^{2L+1} \\ &= 6.02N + 1.76 - 10\log\frac{p^{2L}}{2L+1} + 20\left(L+0.5\right)\log OSR \end{aligned} \tag{5-15}$$

It can be shown that an *Lth*-order noise-shaping modulator improves the *SNR* by *6L+3* dB/octave, equivalent to *L+0.5* bits/octave. However, cascading the integrators in a ΣΔ modulator encounters instability problem. Practically, a maximum number of 4 integrators are used for a higher order ΣΔ modulator.

## 5.3 SC IMPLEMENTATION OF A SD MODULATOR

ΣΔ modulators are usually discrete-time systems and well-matched with SC architectures. In the other words, integrators in ΣΔ converters are most often implemented using fully-differential SC circuits. Figure 5.5 demonstrates a fully-differential SC implementation of a first-order ΣΔ modulator with a 1-bit quantizer.

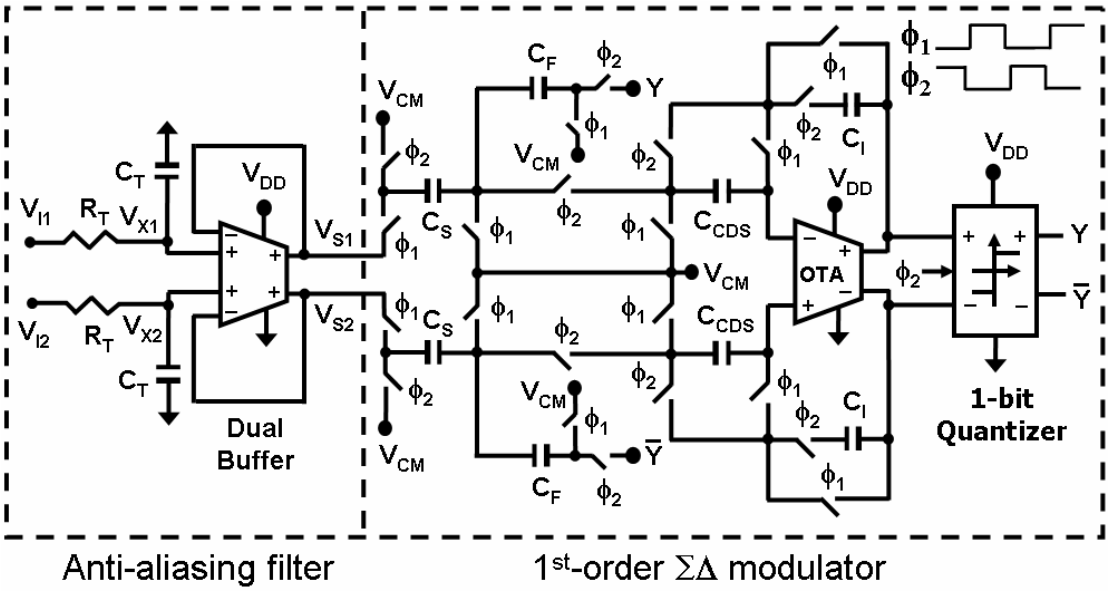
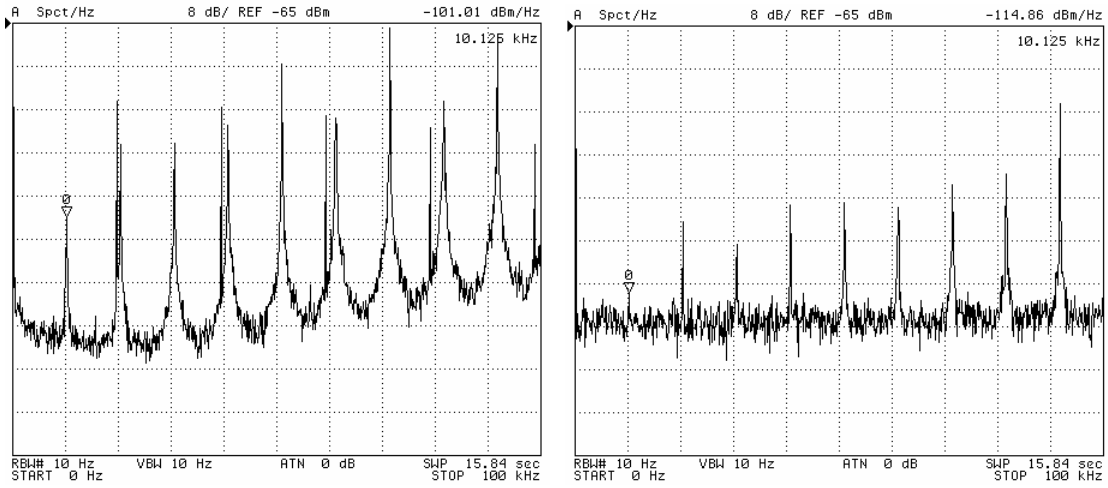



Figure 5.5: An SC implementation of a first-order ΣΔ modulator.

In a fully-differential scheme, even harmonic distortion is not produced by the op amp because its transfer characteristic is symmetric. Also, a fully-differential op amp has a speed benefit over an equivalent single-ended design since it does not have the pole associated with the double-ended to single-ended conversion. However, fully-differential SC circuits require twice the number of capacitors and switches as single-ended counterparts. The capacitor sizes can be halved without affecting the signal-to-thermal-noise ratio of the circuit since the signal swing of the differential circuit is effectively doubled. Therefore, a differential design can occupy the same die area as a

single-ended design. Figure 5.6 clearly shows the effectiveness of the fully-differential scheme in reduction of the environmental interferences. For a powerful spurs at 10 kHz, a 14 dB noise reduction in the differential output of the OTA, introduced in Section 3.5, was measured.




(a) (b)

Figure 5.6: (a) OTA individual output; (b) OTA differential output.

A continuous-time anti-aliasing filter (AAF) prior to the ΣΔ modulator is required to band-limit the input signal to frequencies less than one-half of the oversampling frequency, $f_S$. When the *OSR* is large, the AAF can be a simple *RC* or a *MOSFET-C* low-pass filter. The band-limited continuous signal is processed by the SC integrator of the ΣΔ modulator. The 1-bit quantizer is the last stage and consists of a comparator followed by a transition-gate (TG) D-flip flop (Figure 5.7). The output is latched in the rising edge of $f$, which is the moment to make the decision about the output of 1-bit DAC. In this quantizer, the passing data experiences a delay that should be considered in the *Z*-domain representation of the modulator's transfer function.

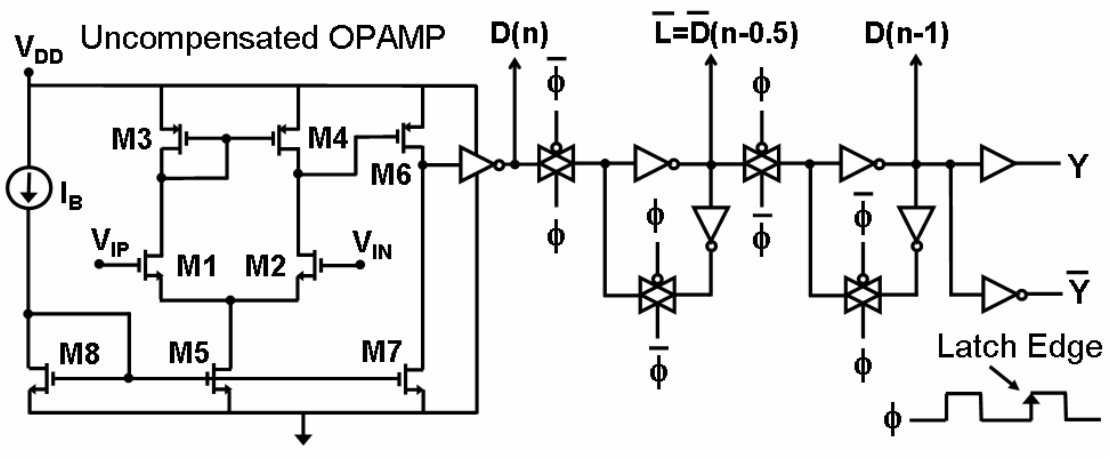



Figure 5.7: Two level clocked-quantizer with delay.

Figure 5.8 shows the *Z*-domain linear model of the first-order ΣΔ modulator presented in Figure 5.5.

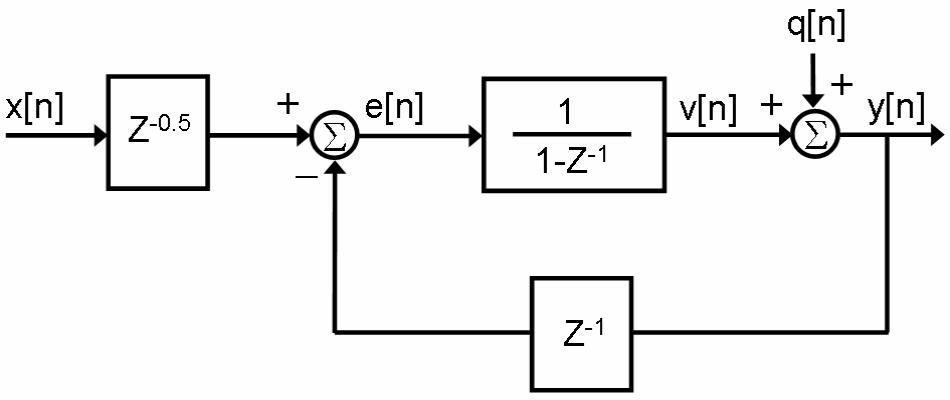



Figure 5.8: *Z*-domain representation of the SC first-order ΣΔ modulator.

The output signal is equal to

$$Y(z) = H_X(z)\,X(z) + H_Q(z)\,Q(z) = z^{-0.5}X(z) + \left(1 - z^{-1}\right)Q(z) \qquad (5\text{-}16)$$

This architecture generates half a delay less in the signal transfer function compared to the architecture presented in Figure 5.2 and has the same noise shaping effect. This implementation delivers 14 bits of resolution with an *OSR* of larger than 500 and 1-bit quantizer.

## 5.4 First-Order SC SD CMOS-SOI Accelerometer

In the previously reported accelerometer ΣΔ interface architectures, the MEMS accelerometer was typically connected to the first stage integrator of a ΣΔ modulator [19] [43] [51] [88]. In contrast, our architecture relies on a front-end charge amplifier and a back-end first-order SC ΣΔ modulator. Figure 5.9 illustrates the functional block diagram of the proposed differential ΣΔ interface IC.

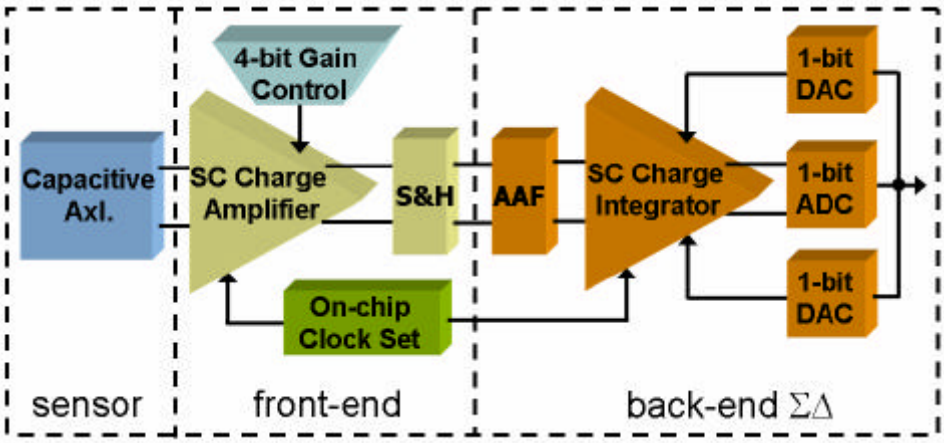



Figure 5.9: Overall building blocks of the proposed fully-differential ΣΔ interface IC.

The main motivation behind the presented architecture is to decouple the ΣΔ modulator from the sensor to achieve optimized performance regardless of the sensor capacitance [72] [74]. With this configuration, the front-end can be clocked at lower frequency. Also, the use of fully-differential configuration reduces the common mode interferences, such as noise coupled through substrate and power line, and increases the dynamic range by 6 dB. Sensors were developed in 40 μm thick low-resistivity (<0.01Ω.cm) SOI wafers through a simple stictionless process that improves the performance and manufacturability of high-sensitivity accelerometers (as presented in Chapter 2). Figure 5.10 shows the schematic diagram of the implemented capacitive SOI accelerometer. The details of fabrication process are provided in Chapter 2.

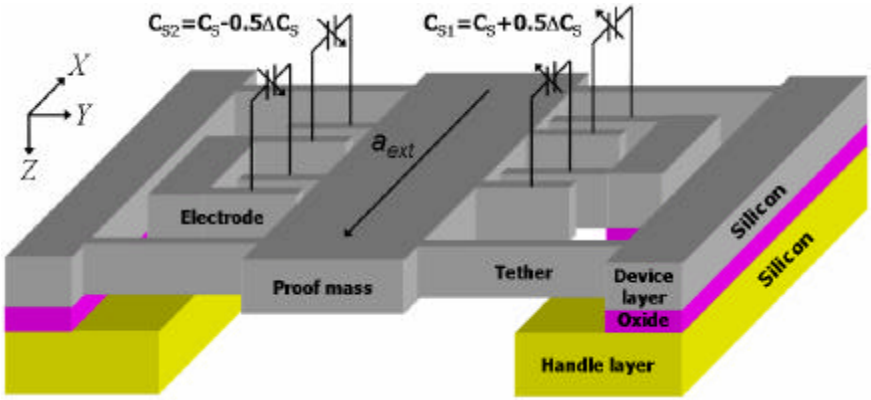
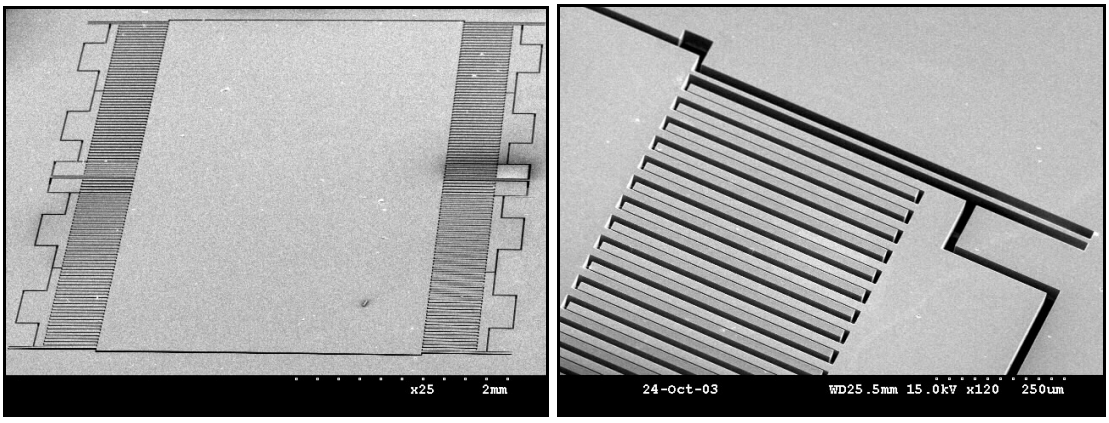



Figure 5.10: Schematic diagram of a capacitive SOI accelerometer.

SEM picture of a fabricated device is shown in Figure 5.11.




(a) (b)

Figure 5.11: (a) SEM of a fabricated dry-released capacitive SOI accelerometer; (b) Close-up view of the tether and sense electrodes.

Design specifications of the SOI accelerometer are provided in Table 5.1.

Table 5.1: Design specifications of a micro-gravity SOI accelerometer.

| | |
|---|---|
| Proof mass size | 4 mm × 3 mm × 40 µm |
| Proof mass | 1.2 milli-gram |
| Capacitive gap size | 2 µm |
| Static sensitivity | 0.2 pF/g |
| Brownian noise floor | 1 µg/√Hz |
| 1st flexural mode | 1.5 kHz |

## 5.5 FIRST-ORDER SD INTERFACE CIRCUIT

Figure 5.12 shows the schematic diagram of the entire interface circuit.

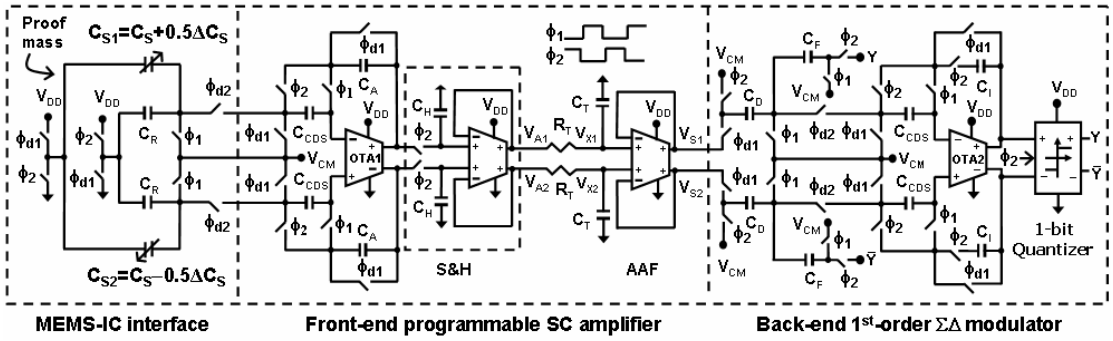



Figure 5.12: Schematic diagram of entire front-end back-end blocks.

The front-end SC charge amplifier converts the changing charge of the capacitive bridge to an amplified voltage, representing the displacement of the proof mass. This sampled signal passes through a sample and hold (S&H) and a simple anti-aliasing filter (AAF) before entering the back-end block. The AAF filters out higher frequency components of the signal to make it more band-limited and to avoid any aliasing problem. The back-end block is a first-order SC ΣΔ modulator that includes an SC voltage integrator followed by a clocked comparator and a 1-bit digital feedback network. In this configuration, the ΣΔ modulator is effectively decoupled from the sensor to achieve optimized performance regardless of the size of the sensor capacitance. In addition, the front-end can be sampled at lower frequency (advantageous when the sensor capacitance and hence the time constants are large), while the back-end is clocked at a higher frequency to up-convert the quantization noise more efficiently. In the following sections, each of the circuit blocks will be described in more details.

### 5.4.1 FRONT-END BLOCK

The front-end block consists of a fully-differential SC charge amplifier followed by a S&H and AAF. The front-end has the versatility of interfacing with different capacitive sensors *($C_{S1,2}$)* and provides an amplified voltage that is converted to a Bitstream through the back-end. The amplification capacitors *($C_A$)* and reference capacitors *($C_R$)* are programmable through a 4-bit digital word. There are two clock phases, $f_1$ & $f_2$, involved in the circuit. In the sampling phase *($f_1$=high, $f_2$=low)*, $C_{S1,2}$ and $C_R$ are charged with $0.5V_{DD}$. Since, in this phase, the output of the OTA is connected to the input node, it is biased properly through the output common mode voltage, therefore a separate input common mode biasing network is not required. Meanwhile, the CDS capacitors *($C_{CDS}$)* accumulate the offset and low-frequency noise. In the amplification phase *($f_1$=low, $f_2$=high*), the accumulated charge in $C_{S1,2}$ and $C_R$ are transferred to $C_A$, and $C_{CDS}$ cancels out the offset and low-frequency noise. Using the charge conservation law between sampling and amplification phases at isolated input nodes of the OTA, one can find the output voltage equal to

$$\Delta V_A = V_{A1} - V_{A2} = \Delta V_A(IDEAL) + \Delta V_A(ERROR) \tag{5-17}$$

where

$$\Delta V_A(IDEAL) = \frac{\Delta C_S}{C_A} V_{DD} \tag{5-18}$$

$$\Delta V_{OA}(ERROR) = \frac{(C_R - C_S)}{(C_S + C_R + C_A)} \frac{\Delta C_S}{C_A} V_{DD} \tag{5-19}$$

The output error voltage is much smaller than the output ideal voltage and it will be zero if $C_R$ is equal to $C_S$ (as a result of programmable reference capacitors). Then the differential output voltage is proportional to $\frac{\Delta C_S}{C_A}$. The S&H at the output of the front-

end block acts as an impulse sampler combined with a comb filter, which interpolates subsequent sampled data and provides a smooth signal [75]. However, the S&H cannot be considered as an AAF since it does not truly band-limit the output signal of the charge amplifier. Therefore, the proceeding AAF band-limits the amplified signal of the front-end before entering the ΣΔ modulator.

### 5.4.2 BACK-END BLOCK

The back-end block consists of an AAF and a first-order ΣΔ modulator which is composed of a fully-differential input/output SC voltage integrator along with a clocked comparator and a negative feedback network. The AAF after the S&H stage is a buffered MOSFET-C low pass filter. The –3dB frequency of the filter is set through MOS transistor sizing. The MOSFETs are biased in the ohmic region and do not generate significant flicker noise. However, the thermal noise generated by MOS resistors is added to the input signal of the ΣΔ modulator and act as a dithering mechanism to randomize the quantization noise spectrum. As provided in Figure 5.13, the comparator measures a slew rate of 30 V/μs, which is more than enough for a sampling clock of 1 MHz that the IC was tested with.

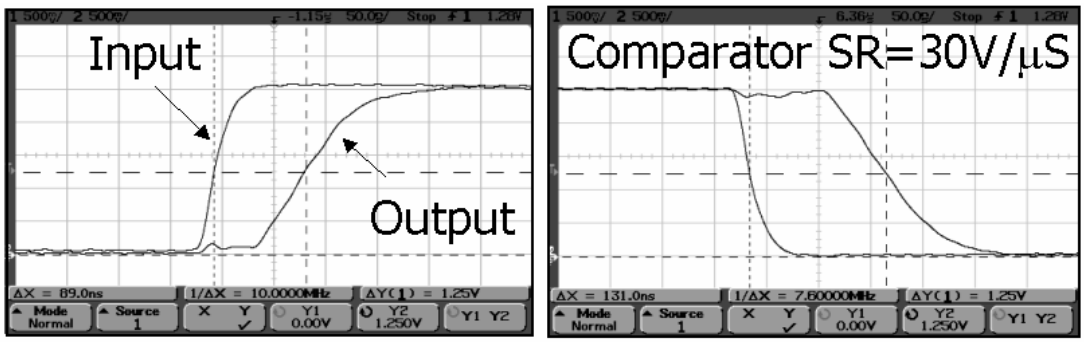
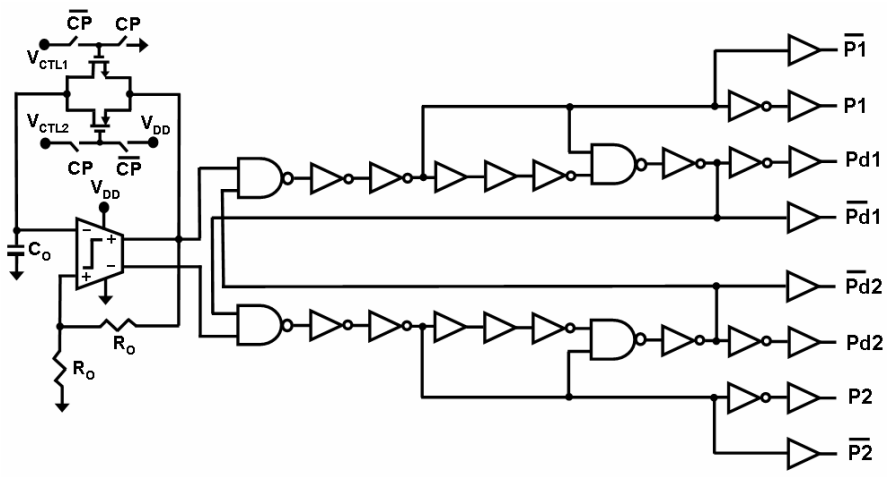



Figure 5.13: Quantizer slew rate measurement results.

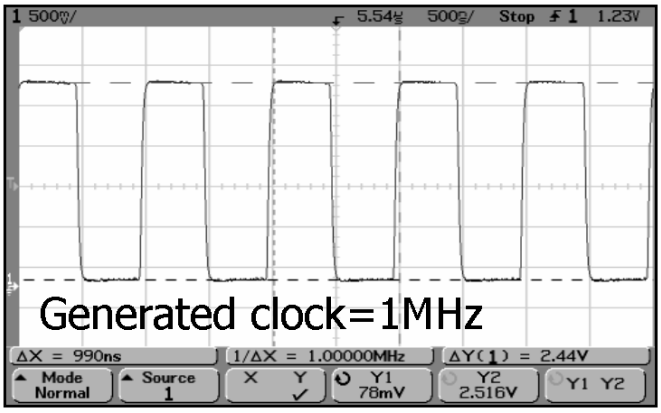
Similar to the front-end block, there are two clock phases, *f1 & f2,* involved in the back-end. In the sampling phase *(f1=high, f1=low)*, $C_D$ is charged with the output voltage of the front-end, and feedback capacitors $(C_F)$ is reset. In the integration phase *(f1=low, f2=high*), the difference between the back-end input signal and 1-bit quantizer output is integrated through the SC voltage integrator and the digital output is latched at the output of the quantizer. There is no need to have programmability for $C_D$, $C_F$ and $C_I$ since the ΣΔ modulator is already isolated from the sensor to maintain the ability of running the back-end even with higher clock frequency. Also, fixing the feedback capacitors saves the chip area. The quantization noise is pushed out of the signal band by introducing the noise shaping transformation or up-converting effect in the integrator loop. The first order SC ΣΔ modulator achieves a quantization noise power of –115 dBm for 100 Hz input acceleration bandwidth and –85 dBm for 1kHz input acceleration bandwidth through a high *OSR*.

### 5.4.3 ON-CHIP CLOCK GENERATOR

A CMOS-controlled relaxation oscillator was designed to generate the on-chip sampling clock and required clock phases as shown in Figure 5.14. Two parallel CMOS transistors $(M_n, M_p)$ are biased in saturation to charge and discharge a capacitor $(C_O)$ with constant current at the negative input of a comparator. The circuit is able to generate variable clock frequency by multiplexing different capacitors at its input. Also for fine tuning of the frequency, two control voltages $(V_{CTL1,2})$ are devised in the oscillator. The two limits of the fast voltage level detector are defined as $0.25V_{DD}$ and $0.75V_{DD}$, which control the charge and discharge of $C_O$.




(a)




(b)

Figure 5.14: (a) CMOS-relaxation oscillator with the multi-phase clock generator; (b) Generated clock pulse at 1MHz and duty cycle of 50%.

To keep $M_n$ and $M_p$ in saturation region, control voltages should stay in the following range:

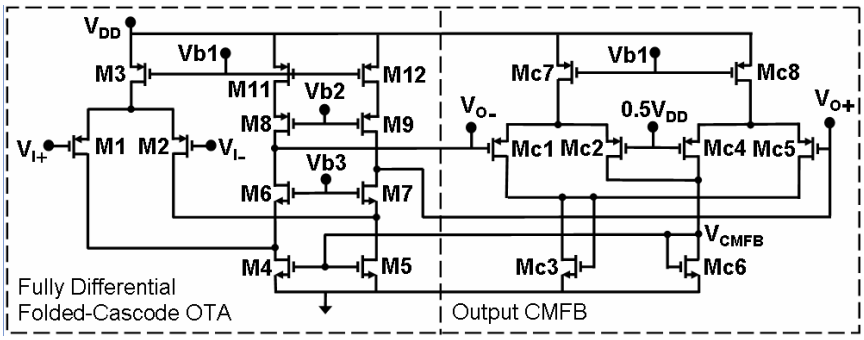
$$V_{TN} \le V_{CTL1} \le \frac{V_{DD}}{4} + V_{TN} \tag{5-20}$$

$$\frac{3}{4}V_{DD} - |V_{TP}| \le V_{CTL2} \le V_{DD} - |V_{TP}| \tag{5-21}$$

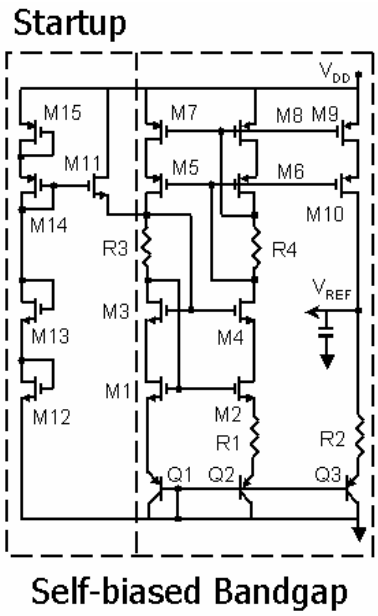
As shown in Figure 5.14(b), the sampling clock frequency was set at 1 MHz with a duty cycle of 50% *($V_{CTL1}+V_{CTL2} = V_{DD}$).*

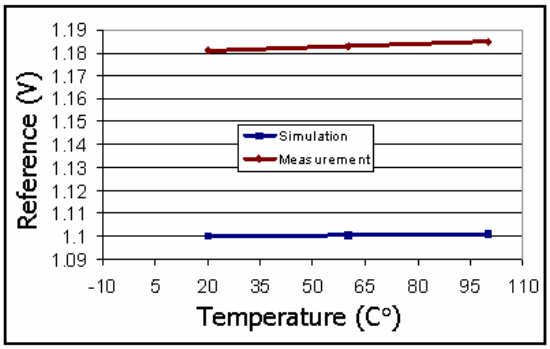
### 5.4.4 LOW-NOISE DESIGN CONSIDERATIONS

The core op amp of the SC charge amplifier and SC integrator is a fully-differential folded-cascode OTA. Figure 5.15(a) shows the transistor level schematic of the implemented OTA including continuous-time common mode feedback (CMFB) circuit.




(a)



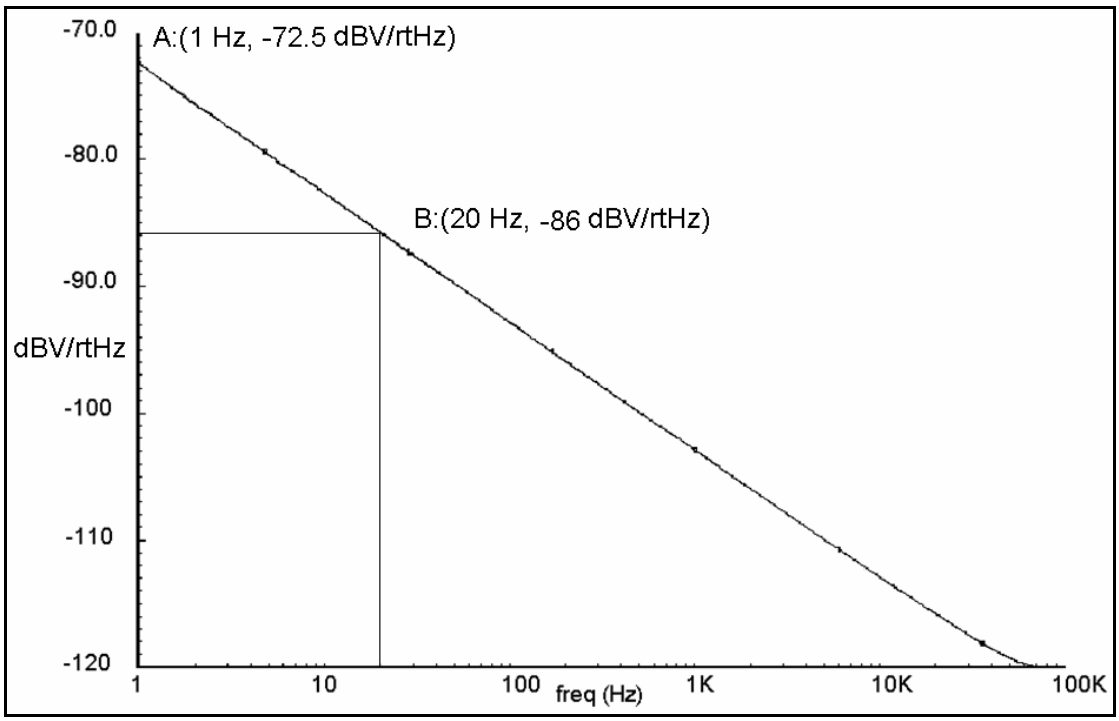

| | Design | Measurement |
|---|---|---|
| $V_{REF}$ | 1.10V | 1.18V |
| T.C. | 15ppm/°C | 40ppm/°C |

(b)

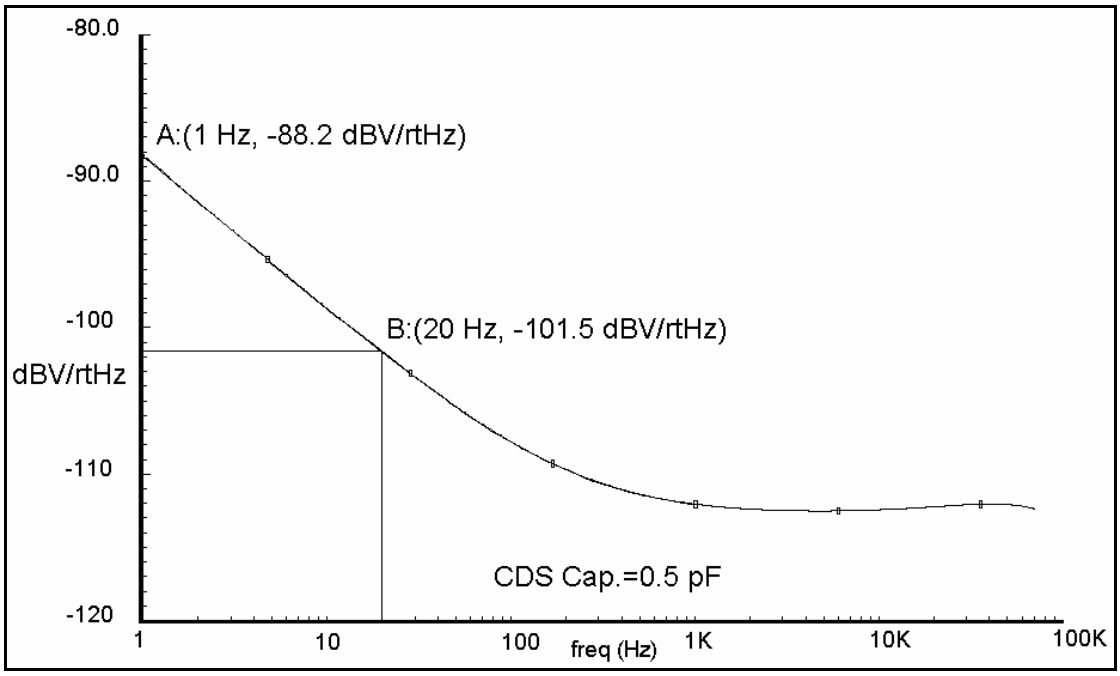
Figure 5.15: (a) A fully-differential folded-cascode OTA; (b) Band-gap voltage reference.

The OTA is self-compensated via the load capacitor. The input referred noise of the OTA is dominated by the noise of transistors $M_1$, $M_2$, $M_4$ and $M_5$. To improve the flicker noise of the OTA, the input stage has large PMOS transistors $(M_1, M_2)$. The transconductance $(g_m)$ of the input transistors are also large enough to avoid noise contribution of other transistors. The biasing voltages $V_{b1}$, $V_{b2}$ and $V_{b3}$ are generated from a bootstrapped current reference that is derived from a band-gap voltage reference as shown in Figure 5.15(b). The measured temperature coefficient (TC) of the band-gap is 40 ppm/°C.

Low frequency noise cancellation is an important requirement in MEMS interfacing, which improves the resolution of the system [22]. In this design, two stages of correlated-double-sampling (CDS) scheme were used in the charge amplifier and ΣΔ integrator for more suppression of the low frequency noise and offset. Figure 5.16 shows the CDS simulation results performed in SPECTRE© using periodic steady state (PSS) and periodic noise (PNOISE) analyses. According to the simulation results a CDS capacitor of 0.5 pF should be able to suppress the noise floor by 16 dB, and the measurement data showed that the CDS technique was eventually able to reduce the flicker noise of the interface IC by 10 dB (Figure 5.17). In this architecture, the front-end charge amplifier not only reduces the noise contribution of the proceeding ΣΔ converter to the overall noise floor of the IC (due to programmable high gain of the charge amplifier), but also adds the ability of interfacing the IC with different accelerometers without compromising the optimized-performance of the ΣΔ modulator.

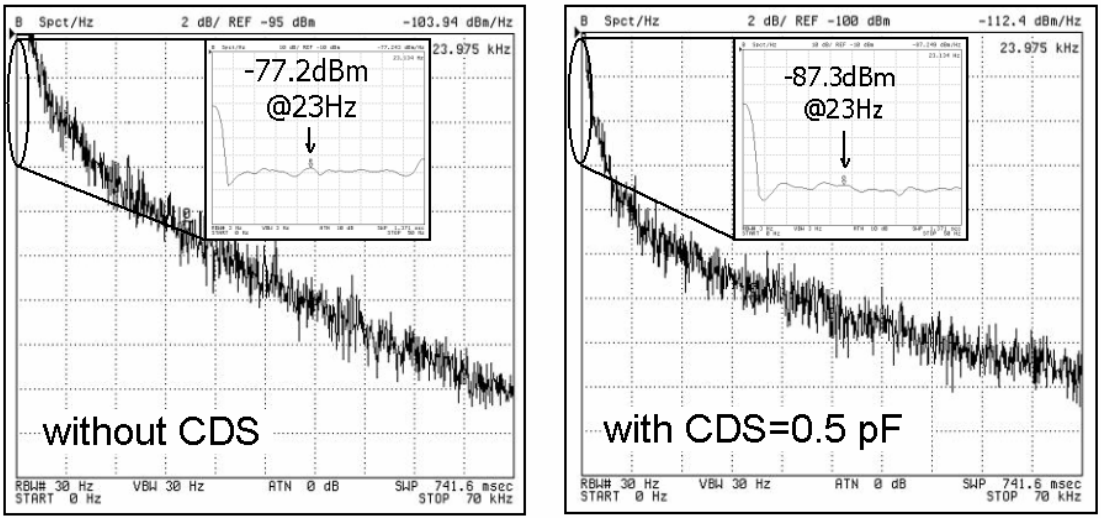



(a)

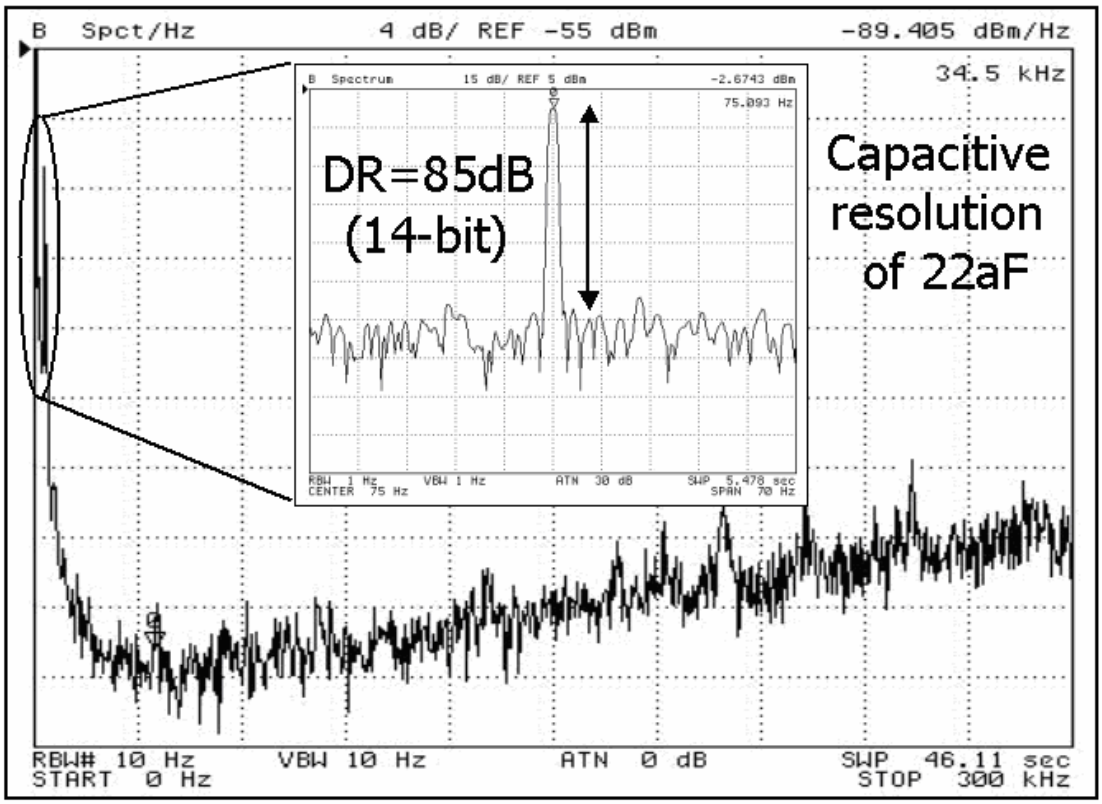



(b)

Figure 5.16: Simulated output noise of the charge amplifier (a) without CDS capacitors; (b) with CDS capacitors *($C_{CDS}$=0.5pF).*




(a)



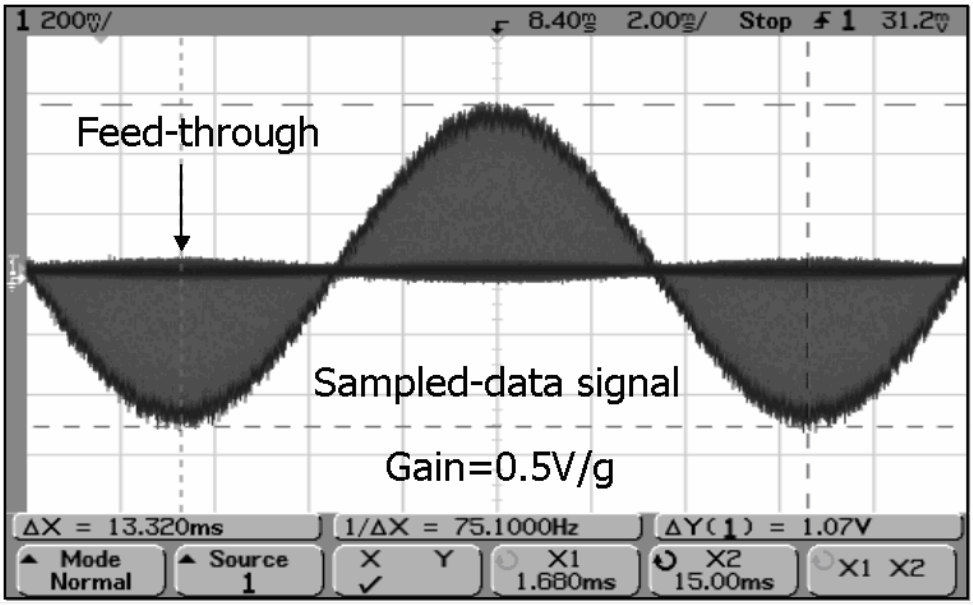

(b)

Figure 5.17: (a) A comparison of the output flicker noise for implementations with and without CDS; (b) Measured up-converted quantization noise spectrum.

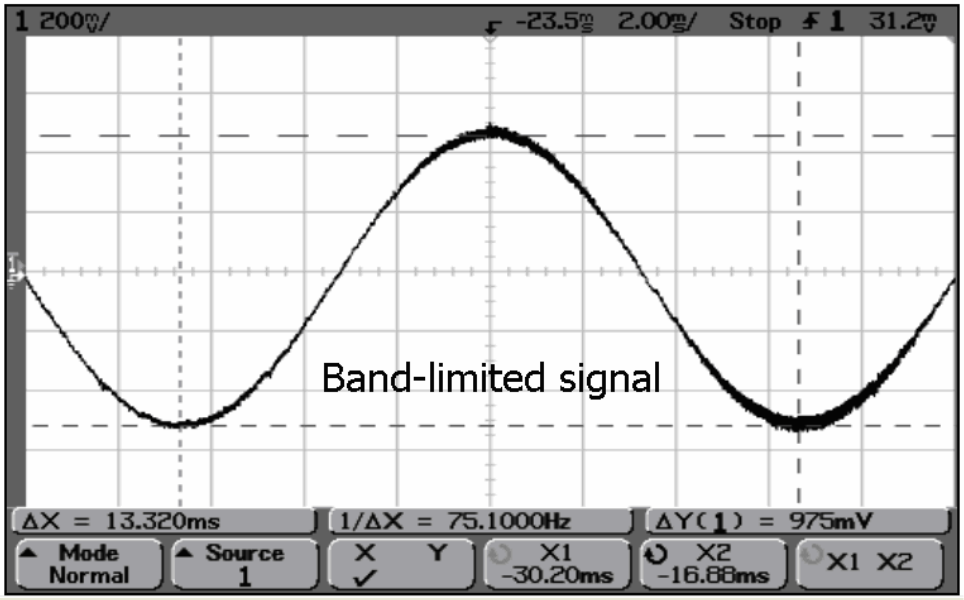
Front-end and back-end blocks each have a dynamic range of 85 dB or larger. Long CMOS switches are used to reduce clock feedthrough and appropriate delayed clocks with their complements are provided to reduce the charge injection of switches. Figure 5.17(b) shows the output noise spectrum of the interface IC, illustrating the noise shaping effect of the modulator and the up-conversion of the quantization noise. The interface IC achieves a dynamic range of 85dB at 75Hz, which is equivalent to a resolution of 14 bits (capacitive resolution of 22aF).

## 5.6 First-Order SD Accelerometer-IC Test Results

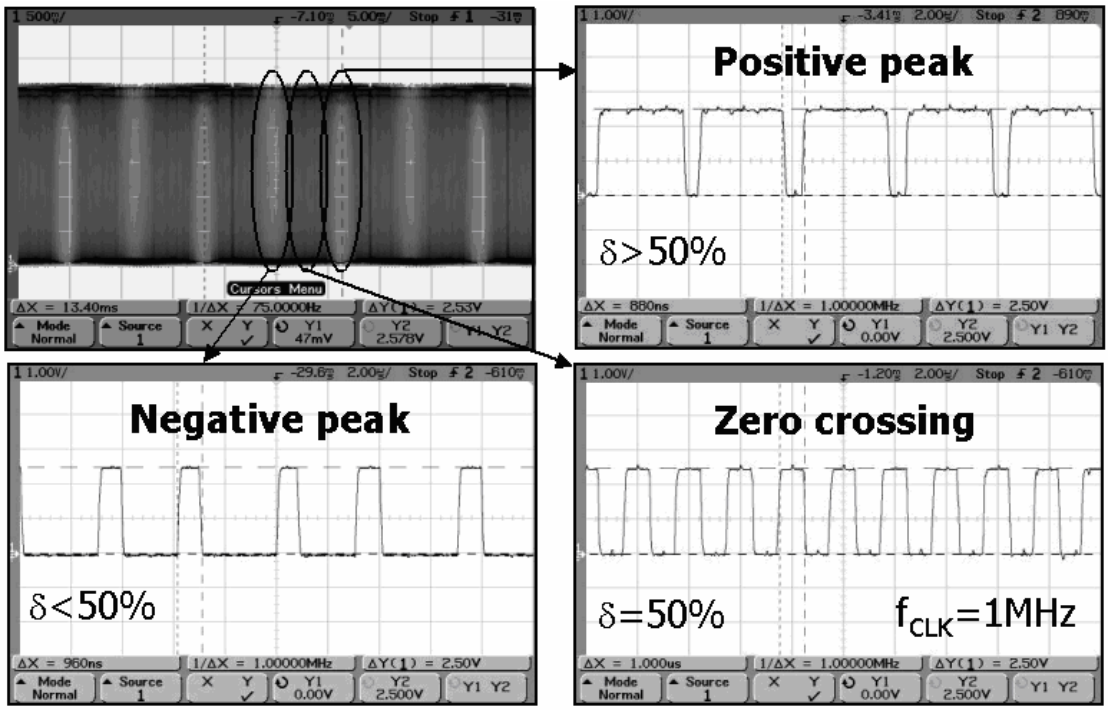
The fabricated SOI accelerometer was wire-bonded to the IC chip. Figure 5.18(a) shows the differential output voltage of the charge amplifier before S&H and AAF. The gain of the amplifier was set to 0.5 V/g and the input acceleration was 1g peak at 75 Hz. There is some feedthrough and charge injection that might cause tone in the output spectrum. Figure 5.18(b) illustrates the front end output voltage after S&H and AAF. The signal is effectively band-limited. This pre-filtering is vital in a ΣΔ modulator. Finally, the 1-bit digital stream is generated at the output of the ΣΔ modulator, and duty cycle of the output pulse is controlled with the level of the input acceleration as shown in Figure 5.18(c). Output duty cycle is larger than 50% for positive acceleration, smaller than 50% for negative acceleration, and 50% for zero crossing acceleration. A shaker diaphragm with a very small displacement was used to generate the sinusoidal acceleration. Also, the differential static response of the accelerometer's front-end block is shown in Figure 5.19 that corresponds to a measured sensitivity of 0.5 V/g.


1 200mV/
8.40ms 2.00ms/ Stop 1 31.2mV
Feed-through
Sampled-data signal
Gain=0.5V/g
ΔX = 13.320ms
1/ΔX = 75.1000Hz
ΔY(1) = 1.07V
Mode Normal
Source 1
X Y
X1 1.680ms
X2 15.00ms
X1 X2

(a)


1 200mV/
-23.5ms 2.00ms/ Stop 1 31.2mV
Band-limited signal
ΔX = 13.320ms
1/ΔX = 75.1000Hz
ΔY(1) = 975mV
Mode Normal
Source 1
X Y
X1 -30.20ms
X2 -16.88ms
X1 X2

(b)




(c)

Figure 5.18: Measured time domain responses to an acceleration of 1g (peak) at 75 Hz; (a) Output of the charge amplifier before S&H and AAF; (b) Output of the charge amplifier after S&H and AAF; (c) ΣΔ output Bitstream.

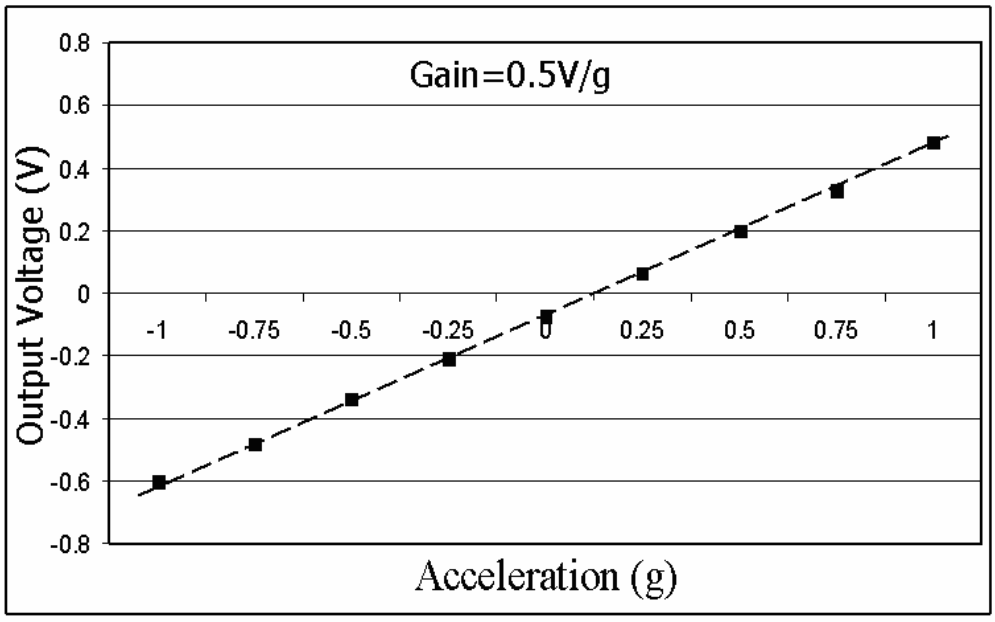



Figure 5.19: Static differential output response to accelerations in the range of ±1g.

The die photo is shown in Figure 5.20. Different blocks of the interface circuit are labeled on the picture.

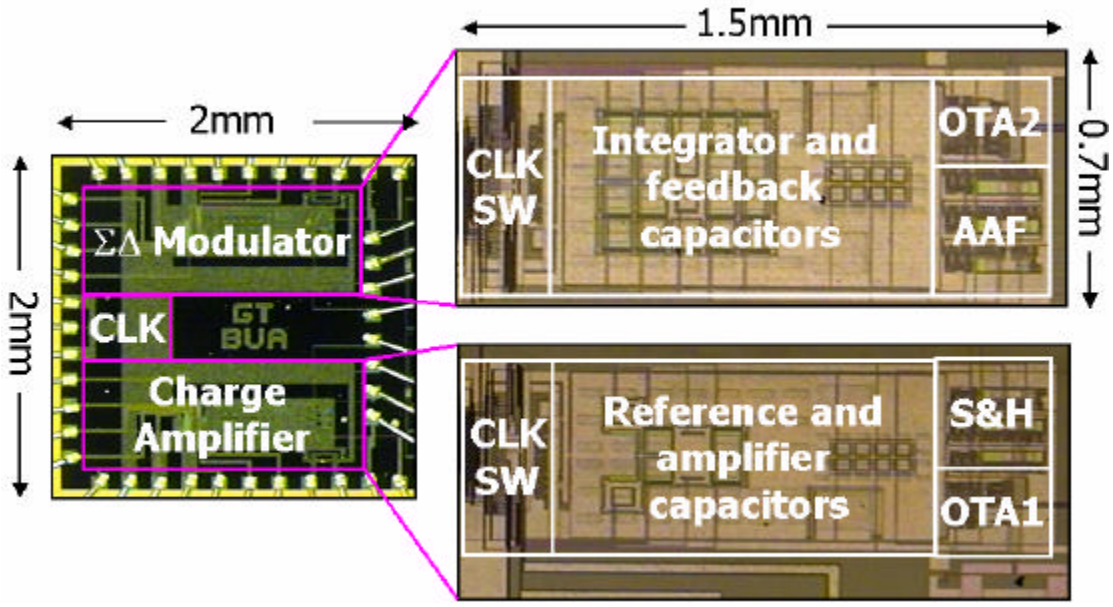



Figure 5.20: Chip microphotograph of the open-loop 2.5 V 14-bit ΣΔ CMOS-SOI accelerometer

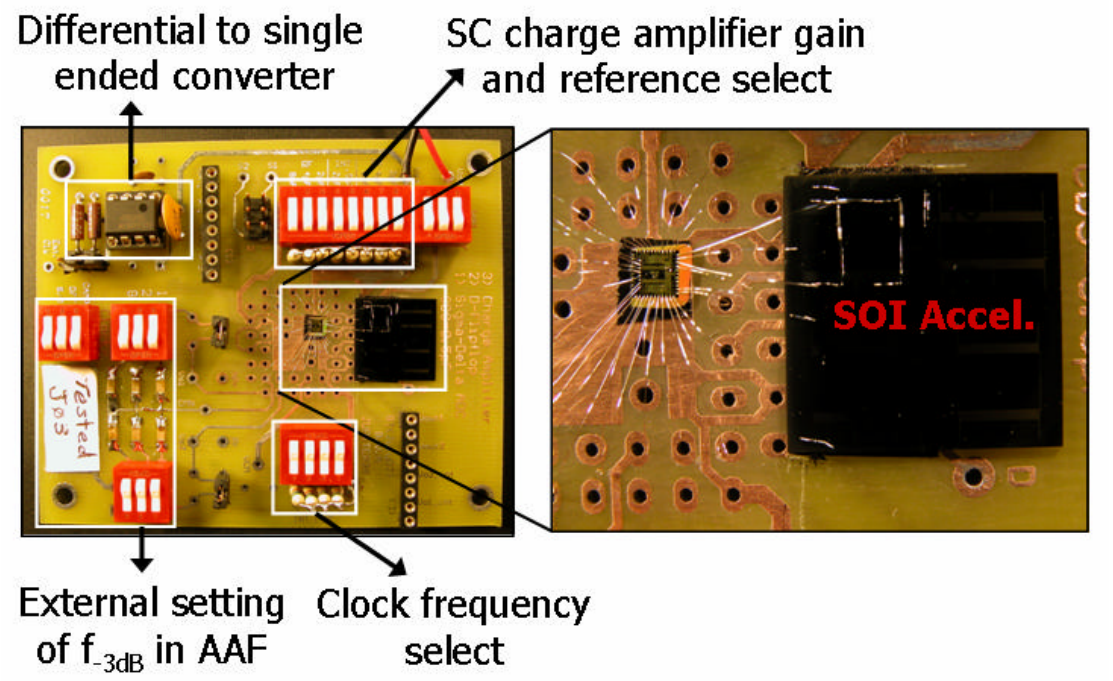



Figure 5.21: Custom-designed PCB to test the ΣΔ CMOS-SOI accelerometer.

The digital portion of the circuit is kept far from the analog circuit to minimize digital noise. Die core area is $2mm^2$ and it is fabricated in the 2.5V 0.25μm 2 poly 5 metal N-well CMOS process from National Semiconductor. Figure 5.21 illustrates the test PCB with the external settings for SC amplifier gain, AAF and clock generator. Summary of the measured specifications of the sensor and the interface IC is provided in Table 5.2.

Table 5.2: Measured specifications of the first-order ΣΔ CMOS-SOI accelerometer.

| **Accelerometer** | |
|---|---|
| Device size | 3.5 mm × 4 mm × 40 μm |
| Rest capacitance *($C_S$)* | 5.3 pF |
| Static sensitivity | 0.2 pF/g |
| BNEA | 1 μg/√Hz |
| Sensor bandwidth | 1.5 kHz |
| **Interface IC** | |
| Technology | 0.25 μm N-well CMOS |
| Power supply | GND-2.5 V |
| Min. detectable acceleration | 110 μg @75 Hz<br>16 μg @10 kHz |
| Capacitance resolution | 22 aF @75 Hz<br>4 aF @10 kHz |
| Dynamic range | 85 dB (equivalent to 14 bits) |
| Gain | 0.5 V/g |
| Sampling clock | 1 MHz |
| Power dissipation | 6 mW |
| Active die area | 2 $mm^2$ |

## 5.8 SUMMARY

The design and implementation of a 2.5 V first-order SC ΣΔ modulator in a 0.25 μm CMOS technology was presented. The interface IC was used to readout a capacitive SOI accelerometer with micro-g mechanical noise floor. The ΣΔ modulator provides a digital bitstream and has the ability of interfacing with different capacitive sensors with an optimized performance. Very high oversampling ratio *(OSR>300)* was key to the effective up-conversion of the output quantization noise in a first-order ΣΔ modulator. The effectiveness of noise cancellation through CDS was quantified by measuring the output noise spectrum of two identical systems, one with and the other without CDS capacitors. Up to 10 dB low frequency noise reduction was measured through CDS without any need for chopper stabilization. The measured equivalent noise acceleration was 110 μg/√Hz and the dynamic range was 85 dB (equivalent to 14 bits of resolution) at 75 Hz.

# CHAPTER 6

# CLOSED-LOOP SD CMOS-SOI ACCELEROMETER

## 6.1 OVERVIEW

A micro-gravity accelerometer should maintain high performance, resolution and stability even at the presence of large background accelerations such as earth gravity. The performance level of open-loop capacitive microaccelerometers is limited in terms of linearity, dynamic range and bandwidth when large background accelerations exist. For a linear operation, the displacement of the seismic mass should be such that secondary effects of air-damping *(D)*, tethers' stiffness *(K)*, and electrostatic forces applied by readout electronics are negligible and do not degrade the overall performance. A low-frequency large input acceleration causes a large displacement that can push the accelerometer into the nonlinear region. Therefore, for a linear operation, the dynamic range is limited. Since the acceleration is a second derivative of the displacement with respect to time, faster movement of the accelerometer (higher input frequency) generates greater acceleration and again causes non-linearity effects. Hence, the operating frequency of an open-loop microaccelerometer is typically smaller than the natural frequency of the sensor (to provide a linear response). A closed-loop configuration or so-called force-rebalancing system, in contrast, reduces such nonlinearities and improves the performance.

In a closed-loop system, the accelerometer sensing element is a part of the loop-gain in the forward path and a feed-back mechanism (actuator) pushes the seismic mass back and keeps the proof mass at its rest position. By maintaining small deflections,

nonlinearities from the mechanical system and electronics interface are minimized. In addition, a high-bandwidth feedback system can extend the measurement bandwidth beyond the natural frequency of the sensor. However, a force-rebalancing accelerometer is not a good solution for low-cost low-sensitivity microaccelerometers since it increases the complexity of the system and the manufacturing cost. For example, in a high-gravity sensor, used for shock and impact detection in an automobile, the applied acceleration is over 10's of g. Therefore, the required feedback force to reposition the proof mass is usually very large and it is not possible to obtain the force in an integrated format. One of the most efficient methods to employ readout/control mechanism in an integrated form is ΣΔ modulation. These modulators provide direct digital output and can be easily integrated within a high density digital CMOS technology [86–88].

The main objective of this chapter is the design and implementation of a new monolithic mixed-signal second-order ΣΔ modulator for the open-loop and closed-loop operation of the integrated micro- & sub-micro-gravity capacitive SOI accelerometers. The proposed microsystem has the versatility of interfacing with sensors of different sensitivity and rest capacitors while maintaining required conversion speed, minimum power consumption (<5 mW), maximum dynamic range (>90 dB) and minimum nonlinearity (<0.1%). Accelerometers are fabricated in thick SOI substrate through the same process discussed in Chapter 2. High capacitive sensitivity eliminates high gain requirement for the front-end amplifier and provides better quantization noise shaping [89]. The interface IC is designed and implemented in the 3 V 0.5 μm 2P3M N-well CMOS technology from AMI. The SOI accelerometer is wirebonded to the IC chip and is tested for the functionality, performance and stability. The actual measurement data is provided.

## 6.2 PRINCIPLE OF OPERATION

The Functional block diagram of a closed-loop capacitive microaccelerometer system is shown in Figure 6.1.

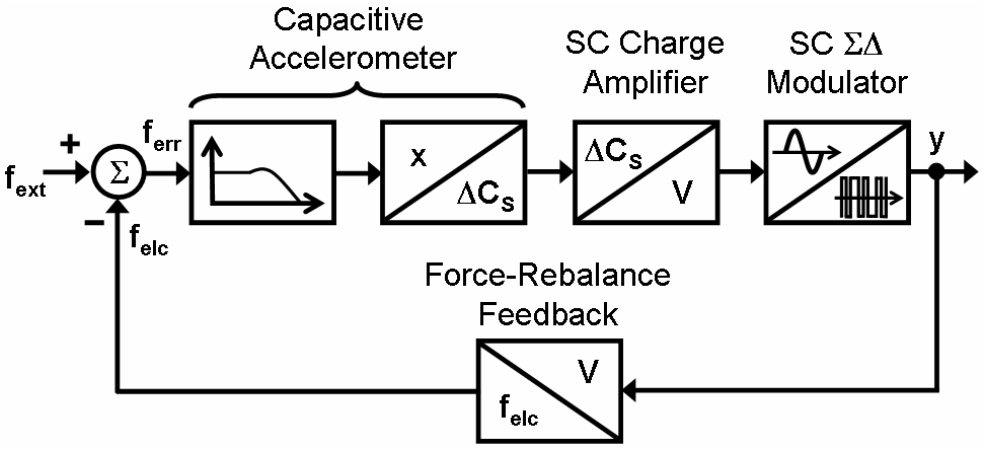



Figure 6.1: Functional block diagram of an electromechanical ΣΔ accelerometer.

The accelerometer includes parallel-plate and comb-drive capacitors around its body (Figure 6.2). The proof mass movement changes the parallel-plate and comb-drive capacitances. The actuator is a part of the accelerometer including comb drives and parallel-plate feedback capacitors.

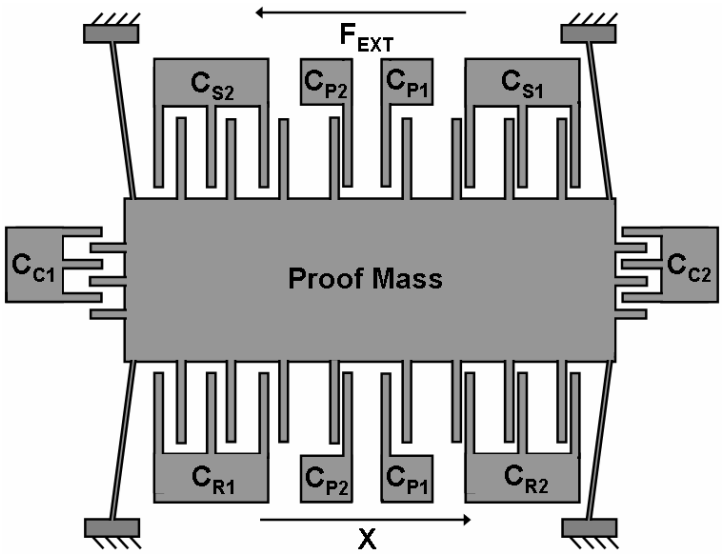



Figure 6.2: Schematic diagram of a capacitive microaccelerometer with parallel-plate sense $C_S$ and comb-drive $C_C$ feedback electrodes.

The value of each changing capacitance is as the following:

$$C_{S1} = \frac{N_e e_0 l_e h}{4(d-x)}, \quad C_{S2} = \frac{N_e e_0 l_e h}{4(d+x)} \tag{6-1}$$

$$C_{R1} = \frac{N_e e_0 l_e h}{4(d+x)}, \quad C_{R2} = \frac{N_e e_0 l_e h}{4(d-x)} \tag{6-2}$$

$$C_{P1} = \frac{N_p e_0 l_e h}{2(d+x)}, \quad C_{P2} = \frac{N_p e_0 l_e h}{2(d-x)} \tag{6-3}$$

$$C_{C1} = \frac{N_c e_0 (l_c - x) h}{2d}, \quad C_{C2} = \frac{N_c e_0 (l_c + x) h}{2d} \tag{6-4}$$

where $N_e$ is the total number of sense electrodes with a length of $l_e$; $N_p$ is the total number of parallel-plate feedback electrodes; $N_c$ is the total number of comb-drive feedback electrodes with initial overlap of $l_c$; $h$ is the height of electrodes; $d$ is the initial gap spacing; $x$ is the proof mass displacement from the rest position. In these equations, $C_{S1}$, $C_{S2}$, $C_{R1}$ & $C_{R2}$ are the sense capacitances, $C_{P1}$ & $C_{P2}$ are the parallel-plate feedback capacitances, and $C_{C1}$ & $C_{C2}$ are the comb-drive feedback capacitances. In force-rebalancing capacitive accelerometer, the error force $(F_E)$ between the external force $(F_{EXT})$ and the feedback force $(F_{ELC})$ passes through the mechanical transfer function of the accelerometer. It has a second-order response with respect to the proof mass displacement $(X)$.

$$M\frac{d^2x}{dt^2} + D\frac{dx}{dt} + Kx = -f_{ext} + f_{elc} = -Ma_{ext} + f_{elc} = -f_{err} \tag{6-5}$$

$$G_{AXL}(s) = \frac{X(s)}{F_{ERR}(s)} = \frac{1}{Ms^2 + Ds + K} \triangleq \frac{G_{AXL0}}{\left(\frac{s}{w_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{w_0}\right) + 1} \tag{6-6}$$

$$w_0 = \sqrt{\frac{K}{M}}, \quad Q = \frac{Mw_0}{D}, \quad G_{AXL0} = \frac{1}{K} \tag{6-7}$$

$w_0$ is the natural angular frequency of the accelerometer, and $Q$ is the quality factor. The differential sense capacitance is equal to

$$\Delta C_S = \frac{1}{2}\left( \frac{N_e e_0 l_e h}{2(d-x)} - \frac{N_e e_0 l_e h}{2(d+x)} \right) = \frac{N_e e_0 l_e h}{2(d^2 - x^2)} x \tag{6-8}$$

For small proof mass displacements, this equation is simplified to

$$\Delta C_S \cong \frac{N_e e_0 l_e h}{2d^2} x = \frac{C_S}{d} x \tag{6-9}$$

$C_S$ is the half of the rest capacitance in between the proof mass sense fingers. The transducer's transfer function is defined as the ratio of output capacitance change over the input force:

$$G_{TDR}(s) = \frac{\Delta C_S(s)}{F_{ERR}(s)} = \frac{C_S}{d} G_{AXL}(s) = \frac{G_{TDR0}}{\left(\frac{s}{w_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{w_0}\right) + 1} \qquad \left[\frac{F}{N}\right] \tag{6-10}$$

$$G_{TDR0} = \frac{C_S}{d}\frac{1}{K} \tag{6-11}$$

The front-end non-inverting SC charge amplifier with a programmable amplification capacitance of $C_A$ picks up the sensor differential capacitance and provides an amplified voltage proportional to the input force

$$V_A(s) = \frac{V_{DD}}{C_A} \Delta C_S(s) = G_{AMP} \frac{G_{TDR0}}{\left(\frac{s}{w_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{w_0}\right) + 1} F_{ERR}(s) \tag{6-12}$$

The converted signal is then band-limited and sampled by two SC integrators that form the second-order ΣΔ modulator with 1-bit digital output. The pulse-width-modulated (PWM) output is amplified and applied to the feedback electrode from which the proof mass is further away, thus generating an electrostatic force to push

the proof mass back to its null position. Feedback electrostatic forces can be generated from parallel-plate electrodes *($F_P$)* or comb drives *($F_C$)*.

$$F_P = -\frac{V_{FB}^{\ 2}}{2}\frac{\partial C_P}{\partial x} = -\frac{V_{FB}^{\ 2}}{2}\frac{\partial\left(\frac{N_p e_0 l_e h}{2(d+x)}\right)}{\partial x} = \frac{N_p e_0 l_e h V_{FB}^{\ 2}}{4d^2}\frac{1}{\left(1+\frac{|x|}{d}\right)^2} \tag{6-13}$$

$$F_C = -\frac{V_{FB}^{\ 2}}{2}\frac{\partial C_C}{\partial x} = -\frac{V_{FB}^{\ 2}}{2}\frac{\partial\left(\frac{N_C e_0 (l_c - x) h}{2d}\right)}{\partial x} = \frac{N_C e_0 h V_{FB}^{\ 2}}{4d} \tag{6-14}$$

The main advantage of the comb-drive actuator over the parallel-plate actuator is that the generated electrostatic force does not depend on the proof mass location and is independent of the comb overlap, while large lateral stiffness of the accelerometer avoids lateral snap of the comb drives. This force is still proportional to the square of the applied feedback voltage *($V_{FB}$)*, which is represented as convolution transformation in the frequency domain. The convolution effect in the feedback loop introduces nonlinearity in the control system. However, the convolution of two identical square waves is equal to the same square wave with squared pulse amplitude, presented as a constant gain in the feedback path. The feedback gain that is applied through the comb-drive actuator is equal to

$$G_{ACT} = \frac{N_C e_0 h V_{FB}^{\ 2}}{4d} \tag{6-15}$$

The proposed interface circuit is a fully-differential sampled-data scheme with the ability of the force-rebalancing feedback. The feedback force is applied to the accelerometer through the comb-drive or parallel-plat actuator. The expected resolution is better than 14 bits. In this study, the tradeoffs between increasing the order of the ΣΔ modulator while lowering the sampling clock and increasing the

oversampling ratio while decreasing the order of the modulator is quantified. Different specifications including power consumption reduction, quantization noise suppression, low-frequency noise reduction, and stability achievement are considered to decide for the best readout/control interface circuit.

## 6.3 CLOSED-LOOP SAMPLED-DATA SYSTEM

In order to design and simulate the electromechanical ΣΔ modulator, it is necessary to first develop a linear control system for the modulator. A linear discrete-time representation is developed for the behavioral modeling of the system. Figure 6.3 shows the block diagram of a sampled-data system. The accelerometer response is continuous-time and the readout/control system is a sampled-data system with discrete-time response. $G_{TDR}(S)$ is the accelerometer's continuous-time transfer function that its output is sampled at regular intervals by an A/D converter.

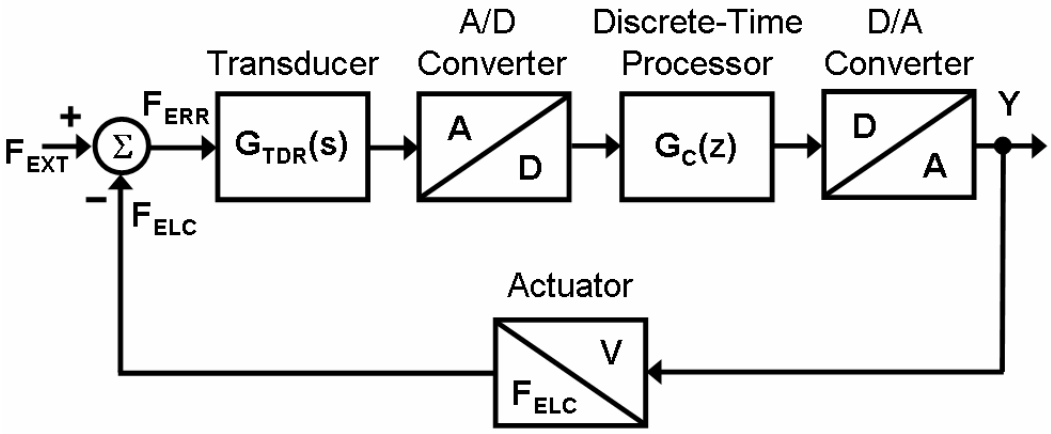



Figure 6.3: Block diagram of a sampled data system.

The role of discrete-time processor is to manipulate a control strategy, which will ultimately be represented as a transfer function in the *Z*-domain $(G_C(z))$. To develop the control algorithm, a precise mathematical model of the overall system (including A/D and D/A converters) is required.

### 6.3.1 CONTINUOUS-TO-DISCRETE TIME CONVERSION

The A/D converter is simply an ideal sampler and consists of an ideal switch that closes and reopens instantaneously every $T_S$ units of time. In modern CMOS IC technologies, CMOS switches are used to implement near ideal samplers. Let *x*(t)* be the sampled-data.

$$x^*(t) = x(t)d_{T_S}(t) \tag{6-16}$$

where *x(t)* is the continuous convolution of *r(t)* and $h_1(t)$ and $d_{T_S}(t)$ is the impulse train function shown in Figure 6.4 and Figure 6.5.

$$x(t) = h_1(t) \otimes r(t) = \int_0^t h_1(t)r(t-t)dt \tag{6-17}$$

$$d_{T_S}(t) \triangleq \sum_{n=0}^{\infty} d(t - nT_S) \tag{6-18}$$

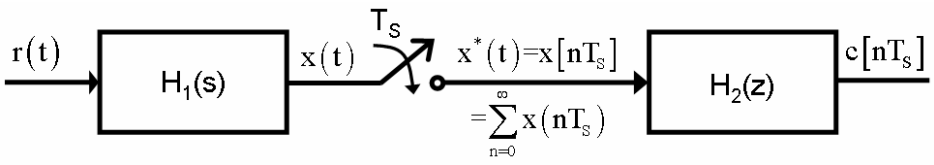



Figure 6.4: Ideal sampler working as a continuous-time-to-discrete-time converter.

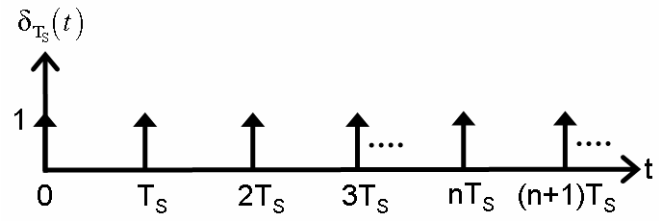



Figure 6.5: Impulse sampler $d_{T_S}(t)$.

Thus, we have:

$$x^*(t) = \int_0^t h_1(t)r(t-t)\,dt \sum_{n=0}^{\infty} d(t - nT_S) = \sum_{n=0}^{\infty} \int_0^t h_1(t)r(t-t)\,d(t - nT_S)\,dt \tag{6-19}$$

The impulse function whose area is equal to unity is called the unity-impulse function or the Dirac delta function and satisfies the following properties:

$$x(t)d(t-t_0)=x(t_0) \tag{6-20}$$

$$\forall\, t\geq o \Rightarrow \int_0^t d(t)dt = \int_{0^-}^{0^+} d(t)dt = 1 \tag{6-21}$$

Therefore,

$$x^*(t)=\sum_{n=0}^{\infty}\int_0^{nT_S} h_1(nT_S)\,r(nT_S-t)\,dt = \sum_{n=0}^{\infty} h_1(nT_S)\otimes r(nT_S)=\sum_{n=0}^{\infty} x(nT_S) \tag{6-22}$$

The definition of *x*(t)* is in-line with the one-sided Laplace transformation used in control systems.

$$X^*(s)=L\{x^*(t)\}=L\left\{x(t)\sum_{n=0}^{\infty} d(t-nT_S)\right\}=\sum_{n=0}^{\infty}\left[\int_{-\infty}^{+\infty} x(t)e^{-st}d(t-nT_S)\,dt\right] \tag{6-23}$$

Replacing Equations (6-20) and (6-21) in Equation (6-23) results in

$$X^*(s)=\sum_{n=0}^{\infty}\left[x(nT_S)e^{-nT_S s}\int_{-\infty}^{+\infty} d(t-nT_S)\,dt\right]=\sum_{n=0}^{\infty} x(nT_S)e^{-nT_S s} \tag{6-24}$$

This Laplace-transfer function is a periodic function.

$$X^*\left(\frac{s\pm j2mp}{T_S}\right)=X^*(s) \tag{6-25}$$

Therefore, any pole or zero of $X^*(s)$ will be repeated every $2p/T_S$. Now, it is easy to present the *Z*-domain transformation since in *Z* transformation, all is needed is replacing $s\rightarrow\frac{Lnz}{T_S}$.

$$X(z)\triangleq X^*(s)\Big|_{s=\frac{1}{T_S}Lnz}=\sum_{k=0}^{\infty} x(kT_S)e^{-kT_S\left(\frac{Lnz}{T_S}\right)}=\sum_{k=0}^{\infty} x(kT_S)z^{-k} \tag{6-26}$$

Here is an example to show how a continuous-time signal is sampled and converted to a discrete-time signal. Let x*(t)* be a damped exponential function for *t>0*.

$$x(t) = e^{-at}U(t) \quad a > 0 \tag{6-27}$$

where *U(t)* is the unit step function:

$$U(t) \triangleq \begin{cases} 1 & t \geq 0 \\ 0 & t < 0 \end{cases} \tag{6-28}$$

The Laplace transform of this function is

$$X(s) = \frac{1}{s+a} \tag{6-29}$$

By using Equation (6-24), the Laplace transform of the sampled-data $x^*(t)$ is equal to

$$X^*(s) = \sum_{n=0}^{\infty} x(nT_S)e^{-nT_S s} = \sum_{n=0}^{\infty} e^{-anT_S}e^{-nT_S s} = \frac{e^{sT_S}}{e^{sT_S} - e^{-aT_S}} \tag{6-30}$$

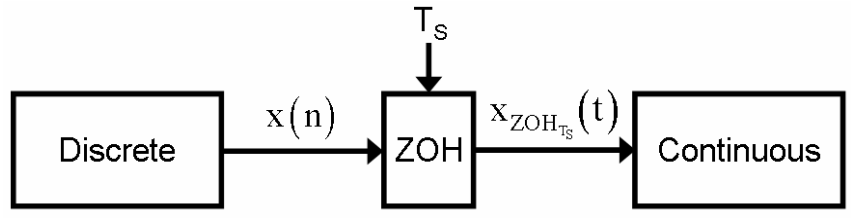
Recalling that $X^*(s)$ is periodic in s-plane, it has accountably infinite number of poles at $s=-a\pm j2np/T_S$, $n=0, 1, 2, ¼$. One of its pole is $s=-a$, the original pole from the continuous function. It is implied that $X^*(s)$ includes the pole of *X(s)* and copies of this pole at intervals of $2p/T_S$. The same argument is true for any other function whose Laplace transform exists. Using the mapping of $s = \frac{Lnz}{T_S}$, $X^*(s)$ is mapped to the *Z*-domain.

$$X(z) = \frac{1}{1 - e^{-aT_S}z^{-1}} \tag{6-31}$$

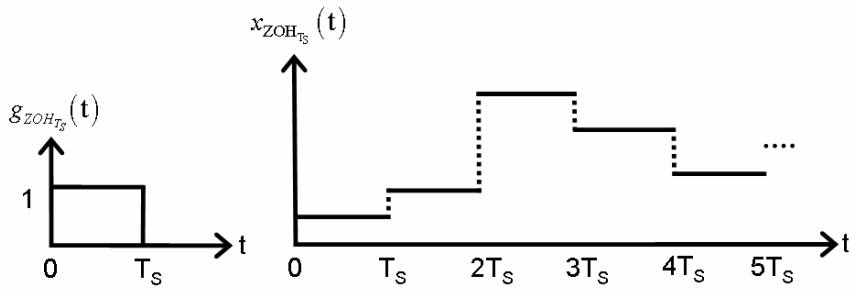
Poles of $X^*(s)$ are obviously mapped to the same point in the *Z*-plane. It is concluded that the poles of *X(z)* are simply the poles of *X(s)* mapped under $z = e^{T_S s}$. The results of this example can be used for any other linear time-invariant (LTI) system in which s-domain transfer functions are ratios of polynomials with real coefficients and can be expanded to partial fractions. However, this rule is not always correct for the zeros.

### 6.3.2 DISCRETE-TO-CONTINUOUS TIME CONVERSION

Next step is to develop a mathematical model for the D/A converter. A zero-order hold (ZOH) is used to turn the discrete signal into a piecewise continuous analog signal, which is applied to the actuator through the feedback-loop. If a unit impulse is applied to the ZOH at *t=0*, the hold mechanism immediately puts out a value of one and hold it for $T_S$ units of time (Figure 6.6). There are many different CMOS sample-and-hold (S&H) or track-and-hold (T&H) circuits to implement the ZOH function.




(a)




(b)

Figure 6.6: (a) Block diagram of an ideal ZOH to model a discrete-to-continuous time converter; (b) Impulse response of a ZOH and a typical output signal of a ZOH.

The Laplace transformation of a ZOH function can be derived as below:

$$g_{ZOH_{T_S}}(t) = U(t) - U(t - T_S) \tag{6-37}$$

where *U(t)* is the unit step function:

$$G_{ZOH_{T_S}}(s) = L\left\{g_{ZOH_{T_S}}(t)\right\} = L\left\{U(t) - U(t\text{-}T_S)\right\} = \frac{1 - e^{-T_S s}}{s} \tag{6-38}$$

Required mathematical equations to manipulate the building blocks of the closed-loop system are now established. Since the models are linear, they can be swept with each other. It was shown that a sampled-data transfer function existed for the control processor. As a result, the entire system can be analyzed in *Z*-domain, and considering Bennett's criteria, linear equations are used to design the electromechanical ΣΔ capacitive SOI accelerometer and study the quantization noise shaping effect.

### 6.3.3 *Z*-DOMAIN PRESENTATION OF THE CLOSED-LOOP SYSTEM

Using the ZOH transfer function, the D/A converter can be swept with the transducer's transfer function. Figure 6.7 shows a new presentation of the closed-loop system where $G_C^*(s)$ represent the discrete-time processor, and $G'_{TDR}(s)$ represent the combination of the ZOH and the transducer's transfer function [90].

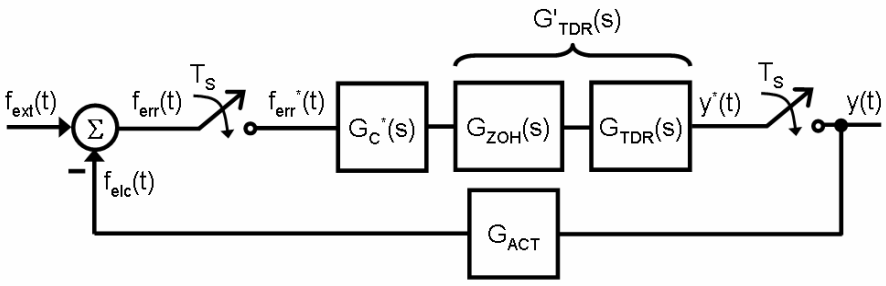



Figure 6.7: Modified block diagram of a closed-loop sampled-data system.

$$G'_{TDR}(s) \triangleq G_{ZOH_{T_S}}(s)\,G_{TDR}(s) = \frac{1-e^{-T_S s}}{s} G_{TDR}(s) \tag{6-39}$$

$$\frac{Y^*(s)}{F^*_{EXT}(s)} = \frac{G^*_C(s)\left[G'_{TDR}(s)\right]^*}{1+G_{ACT}G^*_C(s)\left[G'_{TDR}(s)\right]^*} \tag{6-40}$$

Finally, letting $s \to \frac{Lnz}{T_S}$ in Equation (6-40) yields

$$\frac{Y(z)}{F_{EXT}(z)} = \frac{G_C(z)G'_{TDR}(z)}{1+G_{ACT}G_C(z)G'_{TDR}(z)} \tag{6-41}$$

This equation has exactly the same form as the expression for the closed-loop continuous-time transfer function and can be represented by the block diagram of Figure 6.8.

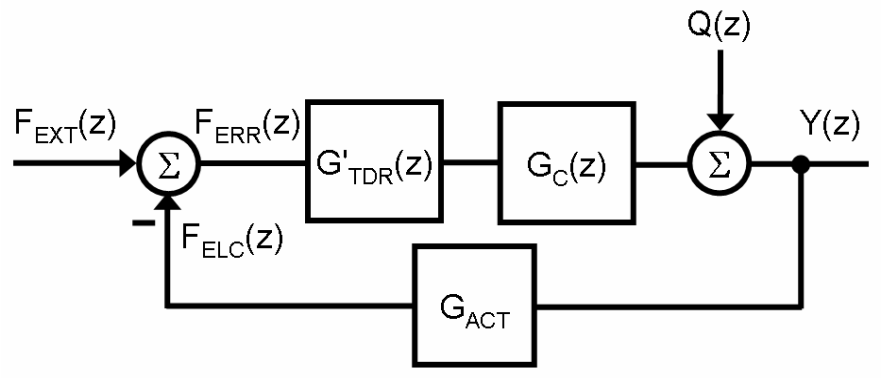



Figure 6.8: Block diagram of a closed-loop sampled data system in the *Z*-domain.

### 6.3.4 *Z*-DOMAIN PRESENTATION OF THE ACCELEROMETER

In this section, a mathematical expression for the $G'_{TDR}(z)$ will be developed. From Equation (6-39), we have:

$$G'_{TDR}(s)=\frac{1}{s}G_{TDR}(s)-\frac{e^{-T_S s}}{s}G_{TDR}(s)=Y_{step}(s)-e^{-T_S s}Y_{step}(s) \qquad (6\text{-}42)$$

where $Y_{step}(s)=sG_{TDR}(s)$ is the *s*-domain expression for the continuous-time response of the transducer to a unit step input. Applying the inverse Laplace transform to $Y_{step}(s)$, the following equation is extracted:

$$g'_{TDR}(t)=L^{-1}\left\{Y_{step}(s)-e^{-T_S s}Y_{step}(s)\right\}=y_{step}(t)U(t)-y_{step}(t-T_S)U(t-T_S) \qquad (6\text{-}43)$$

$U(t)$ is the unit step function. $g'_{TDR}(t)$ is quantized by $t\rightarrow nT_S$.

$$g'_{TDR}(nT_S)=y_{step}(nT_S)U(nT_S)-y_{step}(nT_S-T_S)U(nT_S-T_S) \qquad (6\text{-}44)$$

Then,

$$G'_{TDR}(z) \triangleq \mathrm{Z}\{y_{step}(nT_S)U(nT_S)\} - \mathrm{Z}\{y_{step}(nT_S - T_S)U(nT_S - T_S)\}$$
$$= \sum_{n=0}^{\infty} y_{step}(nT_S)U(nT_S)z^{-n} - \sum_{n=0}^{\infty} y_{step}(nT_S - T_S)U(nT_S - T_S)z^{-n} = (1 - z^{-1})Y_{step}(z) \quad (6\text{-}45)$$

Therefore, the *Z*-domain transform of the accelerometer combined with the ZOH is equal to $(1 - z^{-1})Y_{step}(z)$. $G'_{TDR}(z)$ is called the step-invariant transform of $G_{TDR}(s)$, which is a result of the defined model for D/A converter. The D/A converter has been modeled as a sample-and-hold and a very specific form for $G_{TDR}'(z)$ has been derived. However, the D/A converter can be modeled in a different way (such as first-order hold), and a different formula for $G'_{TDR}(z)$ is obtained. This result is used to transfer the accelerometer to the *Z*-domain. The actuator's transfer function is rewritten as

$$G_{TDR}(s) = \frac{G_{TDR0}}{\left(\frac{s}{w_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{w_0}\right) + 1} = \frac{G_{TDR0}\left(a^2 + b^2\right)}{(s+a)^2 + b^2} \quad where \quad a = \frac{w_0}{2Q},\ a^2 + b^2 = {w_0}^2 \quad (6\text{-}46)$$

$G'_{TDR}(s)$ is found by taking the step-invariant transform of $G_{TDR}(s)$:

$$Y_{step}(s) = \frac{G_{TDR0}\left(a^2 + b^2\right)}{s\left[(s+a)^2 + b^2\right]} \quad (6\text{-}47)$$

Using the standard tables of z transform, $G'_{TDR}(z)$ is found as

$$G'_{TDR}(z) = \frac{G_{TDR0}(Az + B)}{z^2 - \left(2e^{-aT_S}\cos bT_s\right)z + e^{-aT_S}} \quad where \begin{cases} A = 1 - e^{-aT_S}\cos bT_S - \frac{a}{b}e^{-aT_S}\sin bT_S \\ B = e^{-2aT_S} + \frac{a}{b}e^{-aT_S}\sin bT_S - e^{-aT_S}\cos bT_S \end{cases} \quad (6\text{-}48)$$

MATLAB© simulation is used to test the correctness of these equations.

## 6.4 SECOND-ORDER SD CMOS-SOI ACCELEROMETER

In chapter 5.2, it was shown that an open-loop second-order ΣΔ modulator with unity-gain integrators resulted in a second-order noise shaping. Figure 6.9 shows a switched-capacitor implementation of such a system with the same quantizer that was illustrated in Figure 5.7.

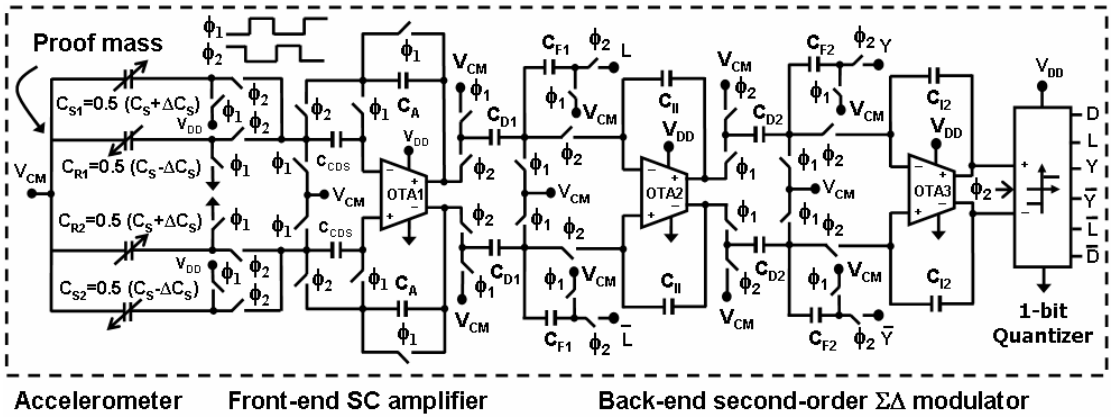
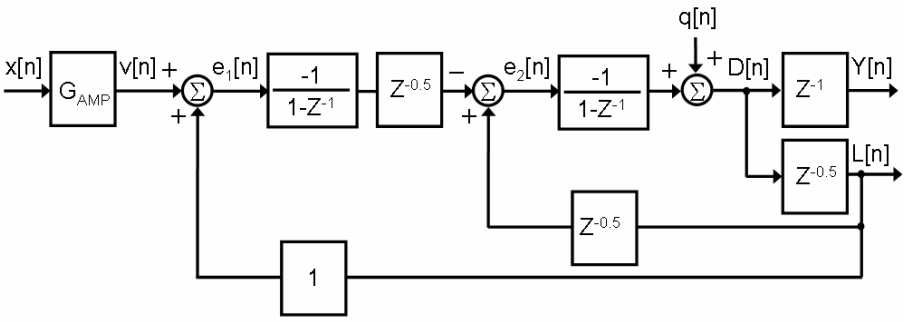



Figure 6.9: Schematic diagram of a second-order ΣΔ readout interface circuit.

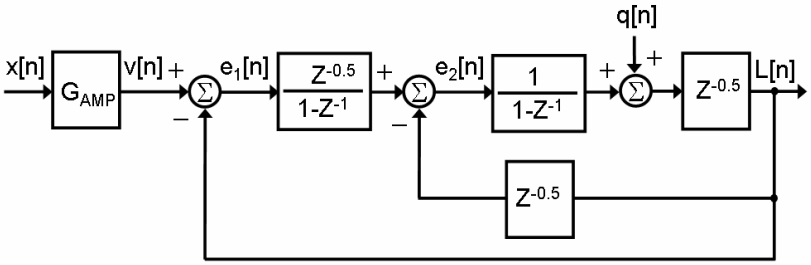
In this schematic, $C_{D1}$, $C_{F1}$, $C_{I1}$, $C_{D2}$, $C_{F2}$, and $C_{I2}$ are equal to set unity gain integrators, and *L[n]=D[n-0.5]* and *Y[n]=D[n-1]* (outputs of the 1-bit quantizer) to provide required delayed feedback levels. Figure 6.10 particularly shows the *Z*-domain linear model of the second-order ΣΔ modulator presented in Figure 6.9. The output signal is equal to

$$L(z) = H_X(z)X(z) + H_Q(z)Q(z) = G_{AMP}z^{-1}X(z) + z^{-0.5}\left(1-z^{-1}\right)^2 Q(z) \quad (6\text{-}49)$$

The second-order quantization noise shaping is achieved with an extra half delay that is negligible for a high *OSR*.




(a)




(b)

Figure 6.10: (a) *Z*-domain representation of the SC second-order ΣΔ modulator; (b) Simplified model.

The second-order ΣΔ interface circuit was simulated by SPECTRE© in CADENCE, with an input of -5 dBm at 100 Hz and a sampling clock of 40 kHz. Figure 6.11 shows the time domain simulation of the designed interface circuit. Also, Figure 6.12 illustrates the power spectral density (PSD) of the 1-bit digital output. The second-order quantization noise shaping reduces the in-band noise to -100 dB at vicinity of input base band (100 Hz). Also, higher order noise shaping helps to reduce the output tones since the output of the first integrator is more chaotic and helps to randomize the quantization noise. Integrators are set for a gain of 0.5 or 1 to provide the maximum noise shaping effect. For low level DC inputs, the outputs of integrators are over-loaded and the circuit shows instability (high power tones). The instability can be avoided by reducing the gain of integrators. The *OSR* is 200 and the calculated quantization noise is -120 dB.

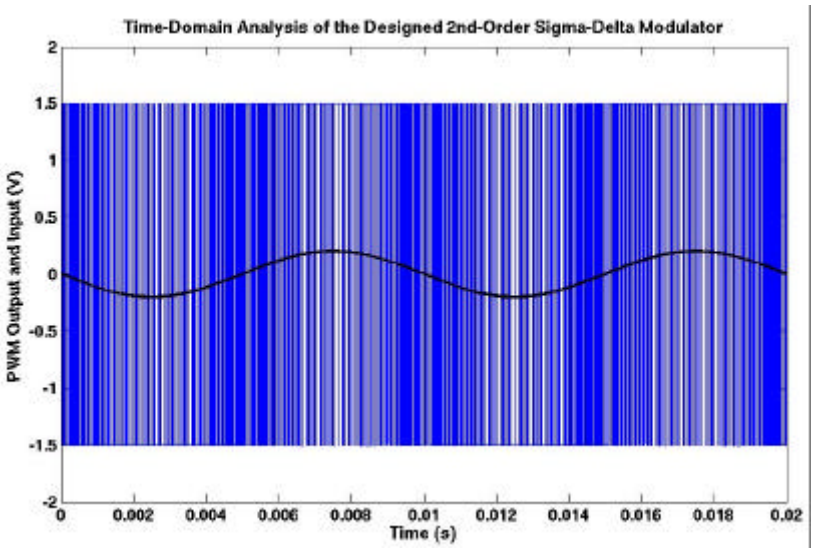



Figure 6.11: Simulated output Bitstream in comparison with the input analog signal.

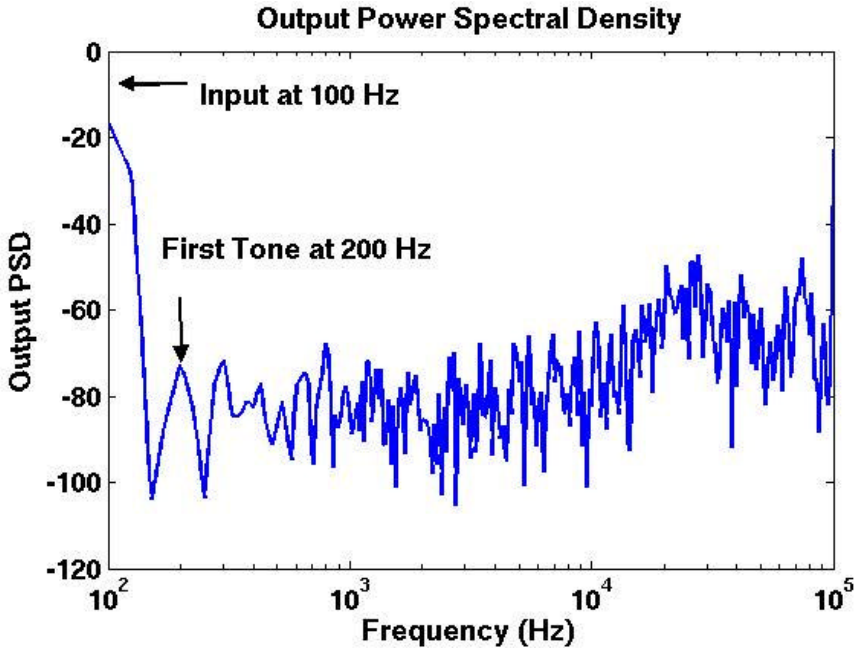
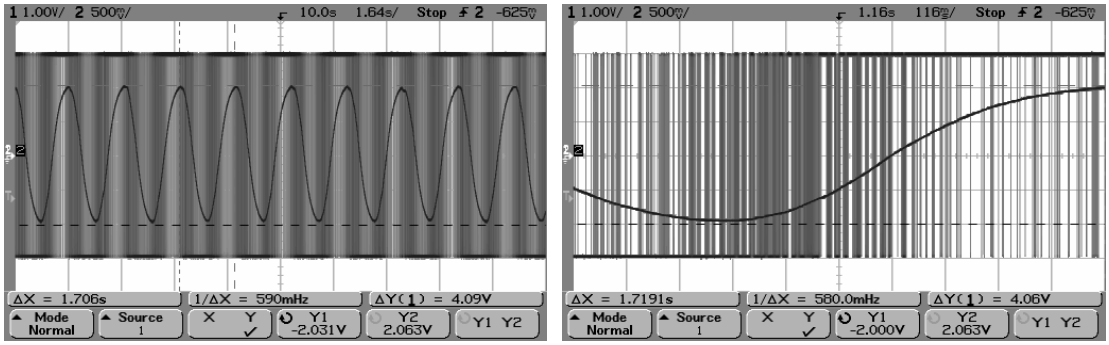



Figure 6.12: Simulated output quantization noise up-conversion.

The real output noise floor is limited by the thermal noise and 1/f noise of the first integrator. The noise of the second integrator is improved through the filtering effect of the first integrator that is placed in the feedback path for the second integrator's input-referred noise. The measured 1-bit digital output of the modulator, for an input acceleration of 30 milli-g at 6 Hz, is illustrated in Figure 6.13.




(a) (b)

Figure 6.13: (a) Measured output Bitstream of the second-order ΣΔ modulator; (b) Close-up view of the PWM signal.

## 6.5 CLOSED-LOOP READOUT/CONTROL SYSTEM

In this section, the design and simulation of the entire closed-loop system is provided. Figure 6.14 illustrates the proposed closed-loop microaccelerometer model using the previously developed mathematical models for the sensor, A/D and D/A converters.

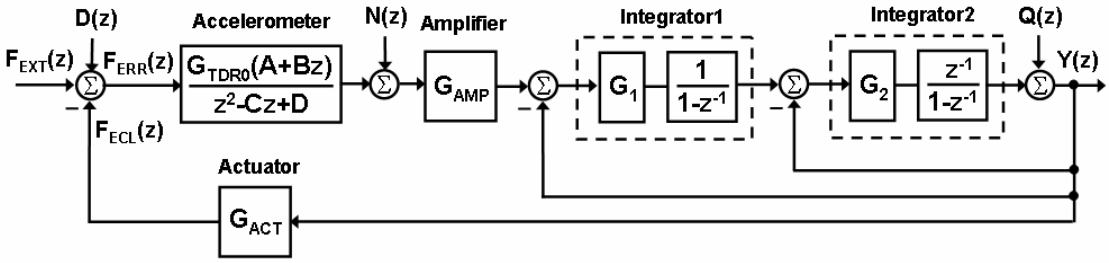



Figure 6.14: Proposed electromechanical ΣΔ modulator in *Z*-domain.

In the closed-loop system, the order of the modulator increases to 4 and instability can cause the modulator to exhibit large cycling states and poor *SNR*. An unstable modulator usually has a low-frequency oscillation that generates an output of alternating long strings of 0's and 1's. Using the linear models presented so far, one can predict if a modulator generates unstable states (limit-cycles). In this configuration, the integrators have separate gains of $G_1$ and $G_2$. The gain of each

integrator can be set through the interface circuit to achieve stability for low-level low-frequency input signals. The step-invariant transfer of the accelerometer is

$$G'_{TDR}(z)=\frac{G_{TDR0}(Az+B)}{z^2-Cz+D} \quad where \begin{cases} A=1-e^{-aT_S}\cos bT_S-\dfrac{a}{b}e^{-aT_S}\sin bT_S \\ B=e^{-2aT_S}+\dfrac{a}{b}e^{-aT_S}\sin bT_S-e^{-aT_S}\cos bT_S \\ C=2e^{-aT_S}\cos bT_s \\ D=e^{-aT_S} \end{cases} \tag{6-48}$$

It is straight forward to find the signal transfer function *(STF)* and the quantization noise transfer function *(QNTF)* from the block diagram of Figure 6.14.

$$STF(z)=\frac{Y(z)}{F_{EXT}(z)}=\frac{G_1G_2G_{AMP}G_{TDR0}(A+Bz)z}{\begin{cases} z^4+(G_2+G_1G_2-C-2)z^3 \\ +\left[1-G_2-C(G_2+G_1G_2-2)+D+G_1G_2G_{ACT}G_{AMP}G_{TDR0}B\right]z^2 \\ +\left[D(G_2+G_1G_2-2)-C(1-G_2)+G_1G_2G_{ACT}G_{AMP}G_{TDR0}A\right]z \\ +(1-G_2)D \end{cases}} \tag{6-49}$$

$$QNTF(z)=\frac{Y(z)}{Q(z)}=\frac{(z^2-Cz+D)(z-1)^2}{\begin{cases} z^4+(G_2+G_1G_2-C-2)z^3 \\ +\left[1-G_2-C(G_2+G_1G_2-2)+D+G_1G_2G_{ACT}G_{AMP}G_{TDR0}B\right]z^2 \\ +\left[D(G_2+G_1G_2-2)-C(1-G_2)+G_1G_2G_{ACT}G_{AMP}G_{TDR0}A\right]z \\ +(1-G_2)D \end{cases}} \tag{6-50}$$

As shown, both of *STF* and *QNTF* have the same poles but the nominator of *QNTF* has the second-order noise shaping multiplied by the denominator of the accelerometer. It means that the transducer's poles are acting as the *QNTF's* zeros. The pole-zero locations of each transfer function depend on the values of the electromechanical coefficients. For a finite impulse response (FIR) transfer function,

the *Z*-domain poles and zeros should locate inside the unity circle and the number of poles should be greater than number of zeros. According to the above equations, the *STF* can conditionally be stable but the existence of repeated zeros on the unity circle can cause *QNTF* to be potentially unstable. The DC gain of each transfer function is found by putting *z=1* (equal to *s=0*).

$$STF_0 = STF(z)\Big|_{z=1} = \frac{\dfrac{G_{AMP}G_{TDR0}(A+B)}{1-C+D}}{1+G_{ACT}\dfrac{G_{AMP}G_{TDR0}(A+B)}{1-C+D}} \tag{6-51}$$

$$QNTF_0 = QNTF(z)\Big|_{z=1} = \frac{0}{1+G_{ACT}\dfrac{G_{AMP}G_{TDR0}(A+B)}{1-C+D}} = 0 \tag{6-52}$$

As it is expected, the *QNTF* has a high-pass characteristic with a second-order null at DC. In addition, at the vicinity of the DC point, the quantization noise is more attenuated by$1+G_{ACT}\dfrac{G_{AMP}G_{TDR0}(A+B)}{1-C+D}$. Obviously, the accelerometer improves the quantization noise shaping, which is one of the main advantages of the closed-loop system.

For the unity gain integrators *($G_1$=$G_2$=1)*, *STF* and *QNTF* are simplified to

$$STF(z) = \frac{Y(z)}{F_{EXT}(z)} = \frac{G_{AMP}G_{TDR0}(A+Bz)z}{z\left(z^3 - Cz^2 + \left(D+G_{AMP}G_{ACT}G_{TDR0}B\right)z + G_{AMP}G_{ACT}G_{TDR0}A\right)} \tag{6-53}$$

$$QNTF(z) = \frac{Y(z)}{Q(z)} = \frac{\left(z^2 - Cz + D\right)(z-1)^2}{z\left(z^3 - Cz^2 + \left(D+G_{AMP}G_{ACT}G_{TDR0}B\right)z + G_{AMP}G_{ACT}G_{TDR0}A\right)} \tag{6-54}$$

For better understanding of the transfer functions effect, the quantitative analysis of the equations is required.

### 6.5.1 DESIGN SPECIFICATIONS OF THE CAPACITIVE ACCELEROMETER

In this section, the accelerometer is first introduced and a sensor transfer function is derived that helps to analyze the closed-loop system. Root Locus is used to predict the stability of the system for different gain values. Figure 6.15 shows the lumped-element model of the capacitive SOI accelerometer.

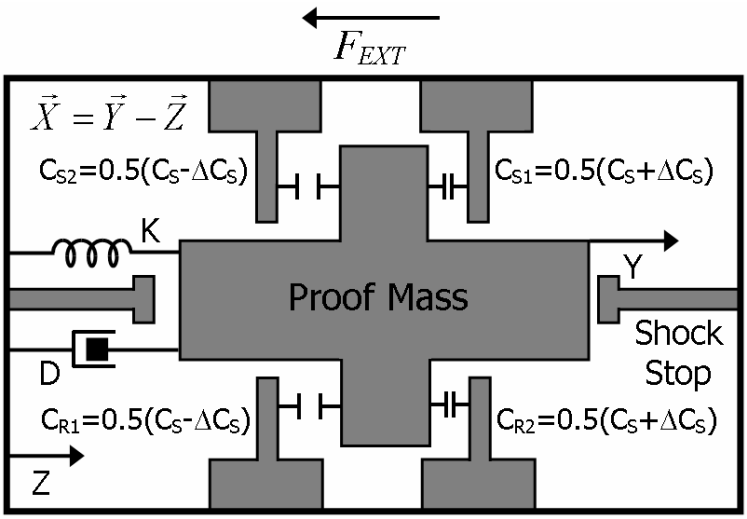



Figure 6.15: Schematic diagram of the SOI microaccelerometer.

Sensors are designed and implemented in thick (120 μm) low-resistivity SOI wafers using the same process flows that were introduced in Chapter 2. Comb-drive actuators are implemented at two ends of the proof mass. The sense capacitance of the accelerometer is split into four identical sub-capacitances in a fully symmetric and differential manner (two increasing and two decreasing) that avoid any on-chip capacitors on the IC. For a non-peaking response, the accelerometer is operated in air and is designed with low quality factor (over-damped response). Figure 6.16 and Figure 6.17 show the capacitive sensitivity and the Brownian noise equivalent acceleration *(BNEA)* of the designed accelerometer with respect to the capacitive gap size.

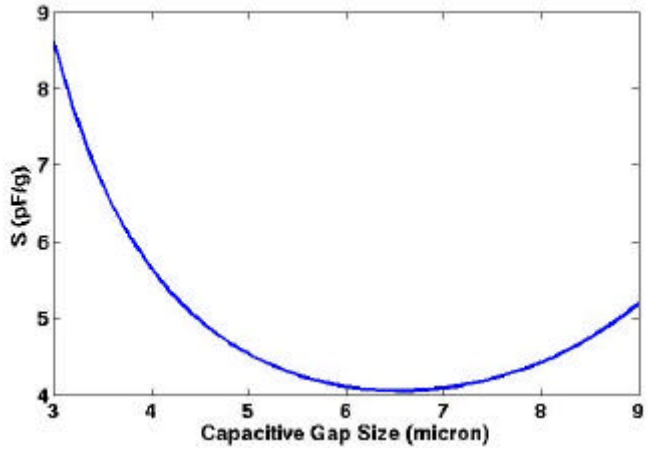



Figure 6.16: Capacitive sensitivity versus gap size.

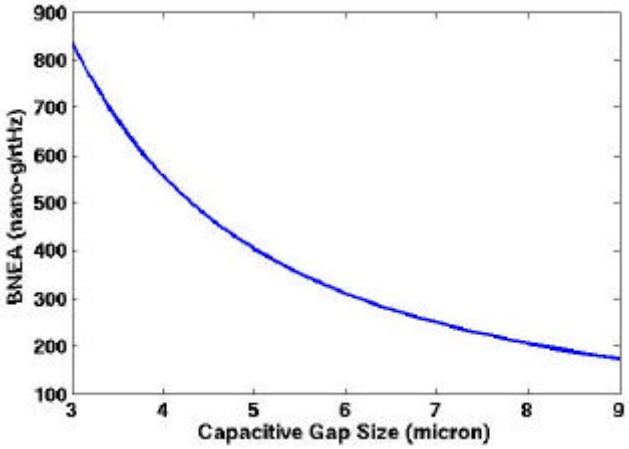



Figure 6.17: *BNEA* versus gap size.

Although the accelerometer is designed for low-*Q* response but it is always difficult to predict and control the actual response of the accelerometer. Therefore, in the control design process, the response of the system for different sensor's quality factors should be analyzed to make sure that changes in the poles location of the transducer will not degrade the performance or cause instability of the system. An ultimate gap of 4 μm is chosen to provide non-peaking response *(Q=0.3)*. Table 6.1 shows the design specifications of capacitive SOI accelerometers.

Table 6.1: Design specifications of the closed-loop micro-gravity SOI accelerometer

| | |
|---|---|
| Proof mass size | 3 mm × 5 mm |
| Overall sensor size | 6 mm × 6 mm |
| Device thickness | 120 μm |
| Initial capacitive gap | 9 μm |
| Reduced gap size | 4 μm |
| Proof mass *(M)* | 5 milli-gram |
| Stiffness *(K)* | 55 N/m |
| Damping *(D)* | $4.5\times10^{-2}$ Ns/m |
| Quality factor *(Q)* | 0.37 |
| $w_0$ | 3.32 krad/s |
| $N_E$ | 120 |
| $N_F$ | 20 |
| $N_C$ | 200 |
| $C_S$ | 12.7 pF |
| *BNEA* | 1 μg/√Hz |
| Static sensitivity *(S)* | 5 pF/g |
| Sensor bandwidth | 550 Hz |
| Maximum input acceleration | 30 milli-g |
| $G_{TDR0}$ | 58 nF/N |
| $G_{ACT}$ | 13.3 nN/V$^2$ *($V_{FB}$=1 V)* |
| $G_{AMP}$ | $6\times10^{12}$ V/F *($C_A$=0.5 pF and $V_{DD}$=3 V)* |
| Dynamic range | >90 dB |

The accelerometer's transfer function is equal to

$$G_{TDR}(s)=\frac{\Delta C_S(s)}{F_{ERR}(s)}=\frac{G_{TDR0}}{\left(\frac{s}{w_0}\right)^2+\frac{1}{Q}\left(\frac{s}{w_0}\right)+1}=\frac{5.8\times10^{-8}}{9.06\times10^{-8}s^2+8.14\times10^{-4}s+1}\quad\left[\frac{F}{N}\right] \tag{6-55}$$

The frequency response of the accelerometer is shown in Figure 6.18.

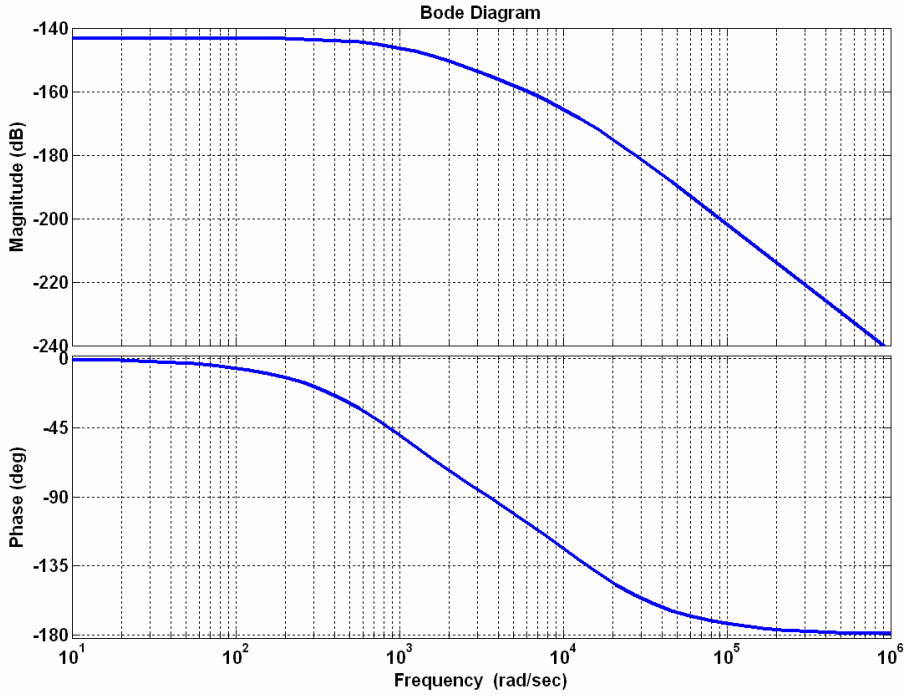



Figure 6.18: Bode plot of the transducer's transfer function.

The designed accelerometer has two real poles at -2π×234 Hz and -2π×1196 Hz and shows no peaking response. For a sampling clock of 40 kHz, the discrete-time transfer function of the accelerometer is

$$G'_{TDR}(z)=\frac{1.792\times10^{-10}z+1.792\times10^{-10}}{z^2-1.793z+0.7988} \tag{6-56}$$

The discrete transfer function of the accelerometer has two real poles at 0.9639 and 0.8287 (inside the unity circle) and a real zero at -1 (Figure 6.19). The accelerometer is stable with the sampling clock of 40 kHz.

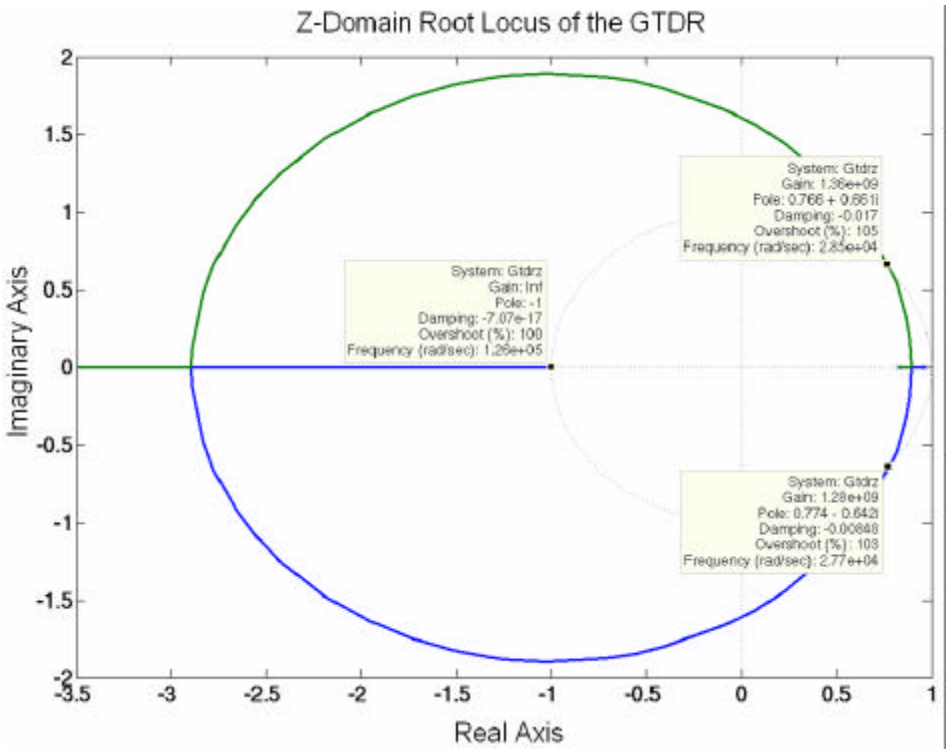



Figure 6.19: Root Locus plot for the step-invariant transform of the accelerometer.

Figure 6.20 illustrates SEM pictures of the fabricated SOI accelerometer for the closed-loop operation. Capacitive gaps are reduced to 4 µm by deposition of 2.5 µm of LPCVD polysilicon over the accelerometer [47]. Shock stops are devised to limit the movement of the seismic proof mass and protect the tethers and sense electrodes from stiction or breaking. In this batch of fabrication, the quality of the deposited polysilicon is improved significantly and a smooth surface is achieved.

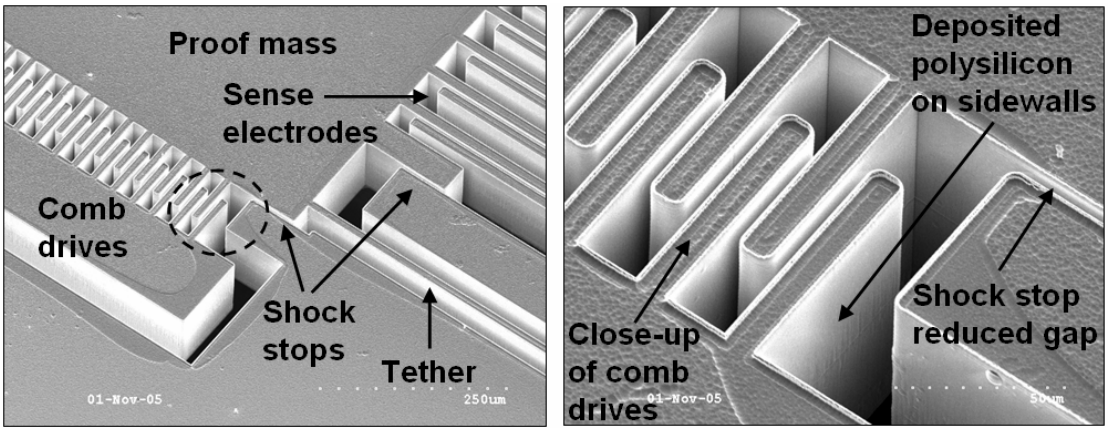



Figure 6.18: SEM pictures of the fabricated SOI accelerometer

### 6.5.2 *Z*-DOMAIN ANALYSIS OF THE ENTIRE CLOSED-LOOP SYSTEM

Each of the blocks in the readout/control system is now defined and we are able to analytically analyze the entire system based on the design specifications. Figure 6.21 depicts the feedback acceleration versus applied feedback voltage *($V_{FB}$)*.

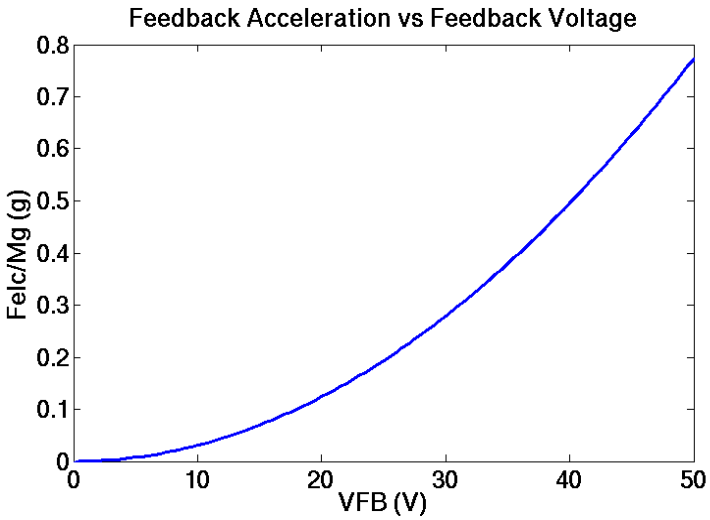



Figure 6.21: Feedback acceleration versus feedback voltage.

The maximum input acceleration for a linear operation is 30 milli-g, which corresponds to a dynamic range *(DR)* of 90 dB, with an acceleration resolution of 1 μg/√Hz. Figure 6.21 predicts that the input acceleration can be increase by 10× (20 dB) if a feedback voltage of 30 V is applied to the comb drives. In the other words, with a feedback voltage of 30 V, the maximum feedback acceleration is 0.3 g, and the accelerometer's respond to the external acceleration *($a_{ext}$)* is linear as long as the error acceleration *($a_{err}$)* is less that 30 milli-g. MATLAB© and SIMULINK© are used to analyze the stability of the closed-loop system and plot frequency responses of the system to the input acceleration, quantization noise and interface circuit noise. For a sampling clock of 40 kHz, feedback voltage of 30 V and unity-gain integrators, the signal transfer function *(STF)*, quantization noise transfer function *(QNTF)*, and the circuit noise transfer function *(NTF)* are as follow:

$$STF(z)=\frac{Y(z)}{F_{EXT}(z)}=\frac{2.88\times10^{-15}z(z+1)(z+6.365\times10^{16})}{z(z+0.00238)(z^2-1.915z+0.9208)} \qquad \left[\frac{V}{N}\right] \qquad (6\text{-}57)$$

$$QNTF(z)=\frac{Y(z)}{Q(z)}=\frac{(z-0.9854)(z-0.9276)(z-1)^2}{z(z+0.00238)(z^2-1.915z+0.9208)} \qquad \left[\frac{V}{V}\right] \qquad (6\text{-}58)$$

$$NTF(z)=\frac{Y(z)}{N(z)}=\frac{6\times10^{12}z(z-0.9854)(z-0.9276)}{z(z+0.00238)(z^2-1.915z+0.9208)} \qquad \left[\frac{V}{F}\right] \qquad (6\text{-}59)$$

The poles and zeros of the transfer functions are placed in side the unity circle that guarantees the stability of the system. The frequency response of each transfer function is shown in the following figures. The dashed curves demonstrate open-loop system *($V_{FB}=0$)* and the solid curves demonstrate the closed-loop system *($V_{FB}=30$ V).*

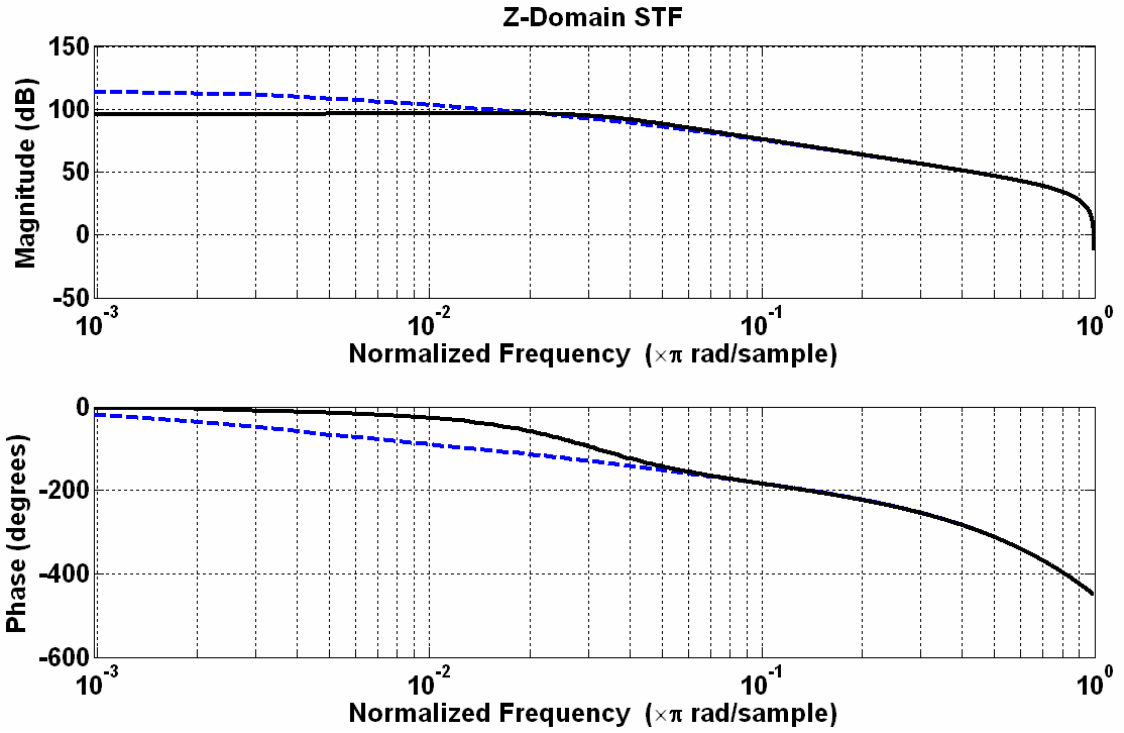



Figure 6.22: *STF* frequency response; Gain is 20 dB reduced in closed-loop system.

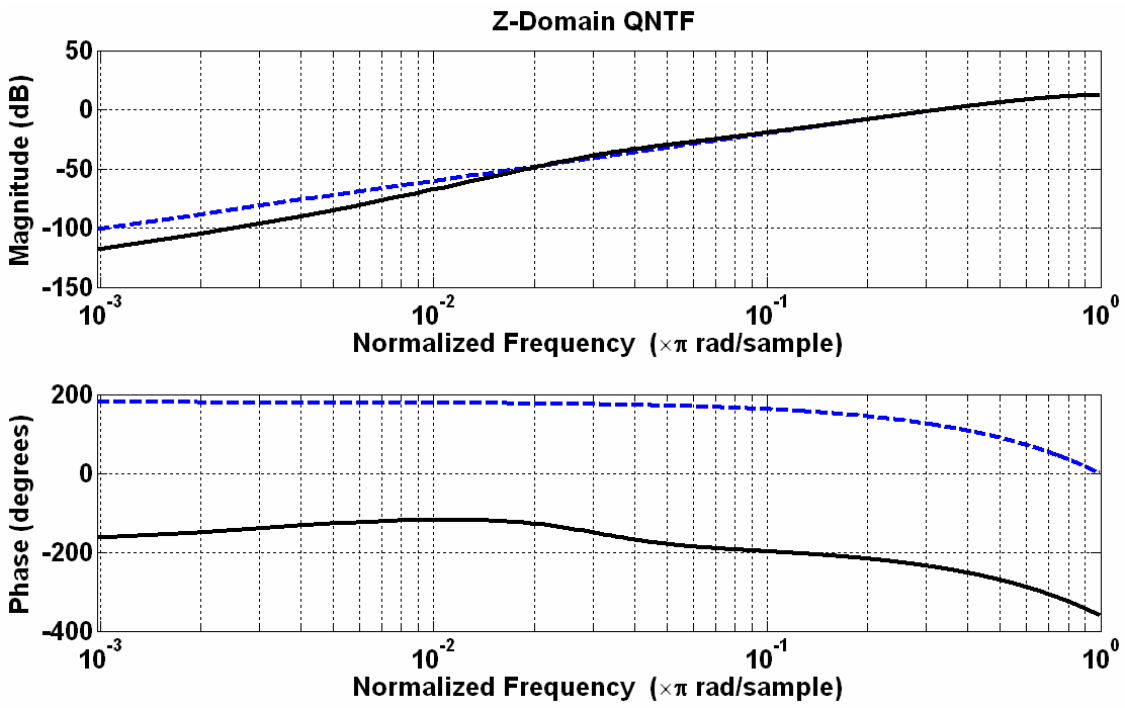



Figure 6.23: *QNTF* frequency response; Quantization noise is improved by 20 dB.

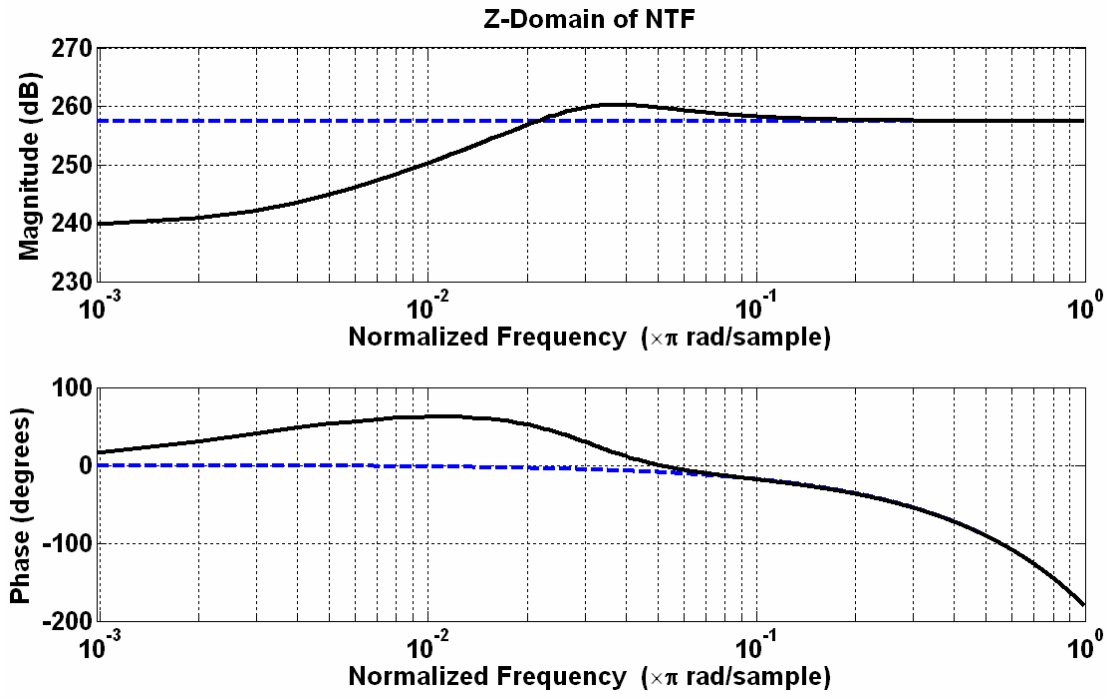



Figure 6.24: *NTF* frequency response; Circuit noise is improved by 20 dB.

As shown in these plots, the *DR* is improved by 20 dB when the accelerometer is in a closed-loop configuration. The quantization noise is up-converted better and is attenuated by 20 dB in the signal bandwidth. In addition, the circuit input referred noise is shaped by the accelerometer transfer function, which helps to maintain the same resolution with the increased dynamic range. Figure 6.25 shows the time-domain step response of the closed-loop system to a 0.3 g external acceleration. The system shows no over-shoot and settles within 1 ms.

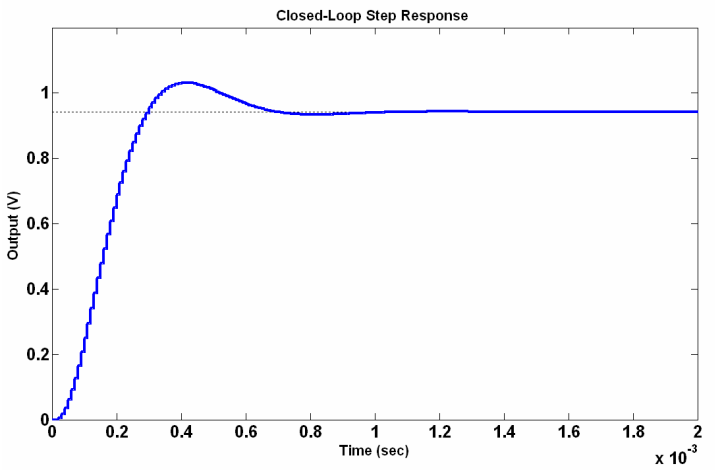



Figure 6.25: Closed-loop microaccelerometer's step response.

## 6.6 CLOSED-LOOP SD CMOS-SOI ACCELEROMETER

In previous sections, the system-level design and simulation of the electromechanical ΣΔ SOI accelerometer was introduced. A linear model of the entire system in *Z*-domain was developed to predict the dynamic range improvement and stability conditions when the accelerometer is placed in the forward path of a closed-loop readout/control system.

Based on the previous analyses, a new monolithic mixed-signal second-order ΣΔ modulator for the closed-loop operation of the micro-gravity SOI accelerometers is presented. This architecture relies on a front-end programmable reference-capacitor-less SC charge amplifier and a back-end second-order ΣΔ modulator, consisting of two cascaded SC integrators with programmable gain of 0.5 or 1, a two-level quantizer and feedback networks. Two comb-drive actuators are dedicated to continuously apply the appropriate feedback force to the proof mass and the output Bitstream controls the average of the applied force. There is no distinct feedback clock phase, which decreases the complexity of the system. Since comb drives are implemented in thick SOI with reduced gap, the feedback force is strong enough to null the movement of the large proof mass.

Correlated-double-sampling (CDS) scheme was used in the front-end to reduce flicker noise and offset. A low-power low-noise fully-differential folded-regulated cascode OTA is designed with a very high DC gain (>100 dB) and a unity gain bandwidth of 4 MHz, as the core op amp in each block. High DC gain of the amplifier improves the SC functionality and noise performance of the system. The closed-loop architecture maintains required converting speed, minimum power consumption (<5 mW), maximum dynamic range (>90 dB) and minimum nonlinearity (<0.1%).

### 6.6.1 INTEGRATED CIRCUIT DESIGN AND SIMULATION

Schematic of the proposed CMOS-SOI ΣΔ accelerometer is shown is Figure 6.26.

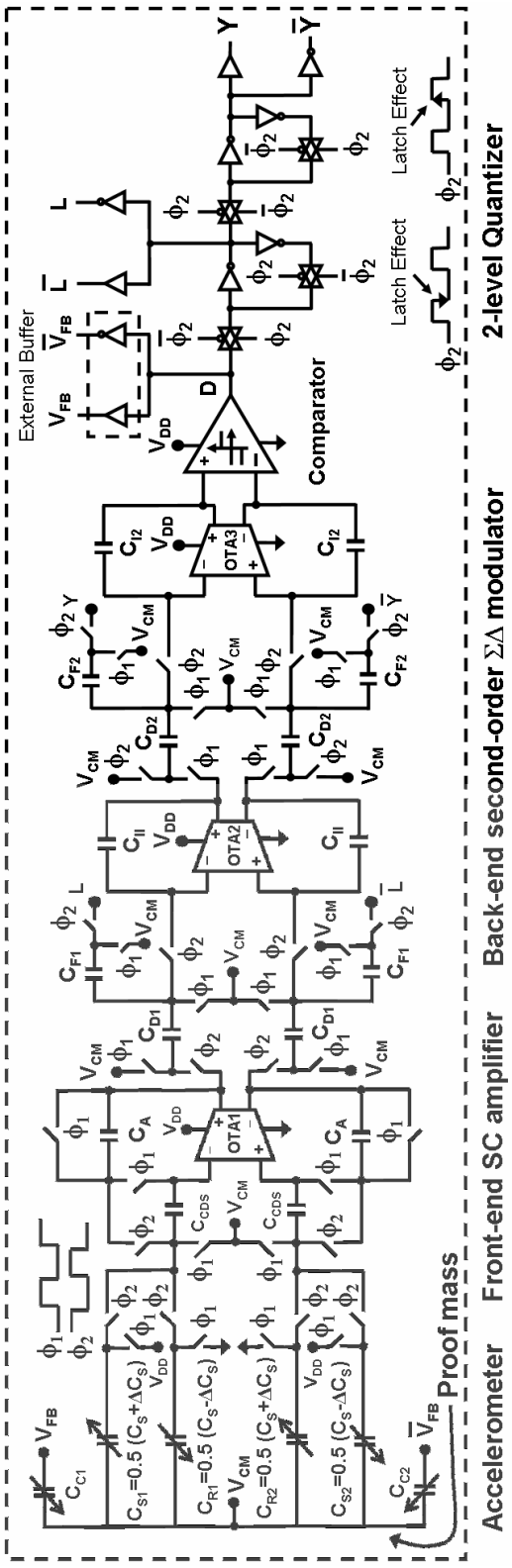



Figure 6.26: Schematic diagram of the electromechanical ΣΔ SOI accelerometer.

For the transistor-level design and simulation of the entire closed-loop system in CADENCE, the accelerometer is modeled with a series *RLC* circuit as shown in Figure 6.27.

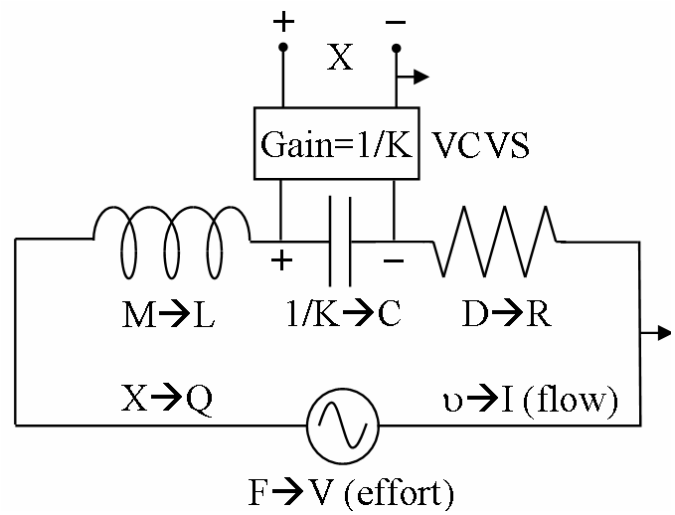
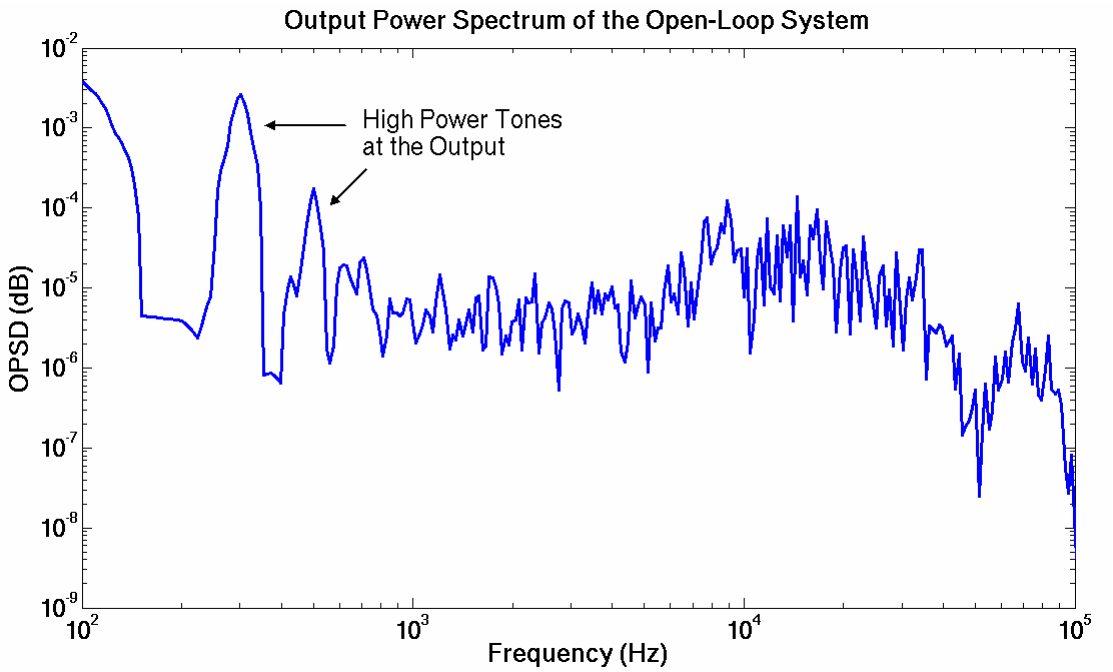


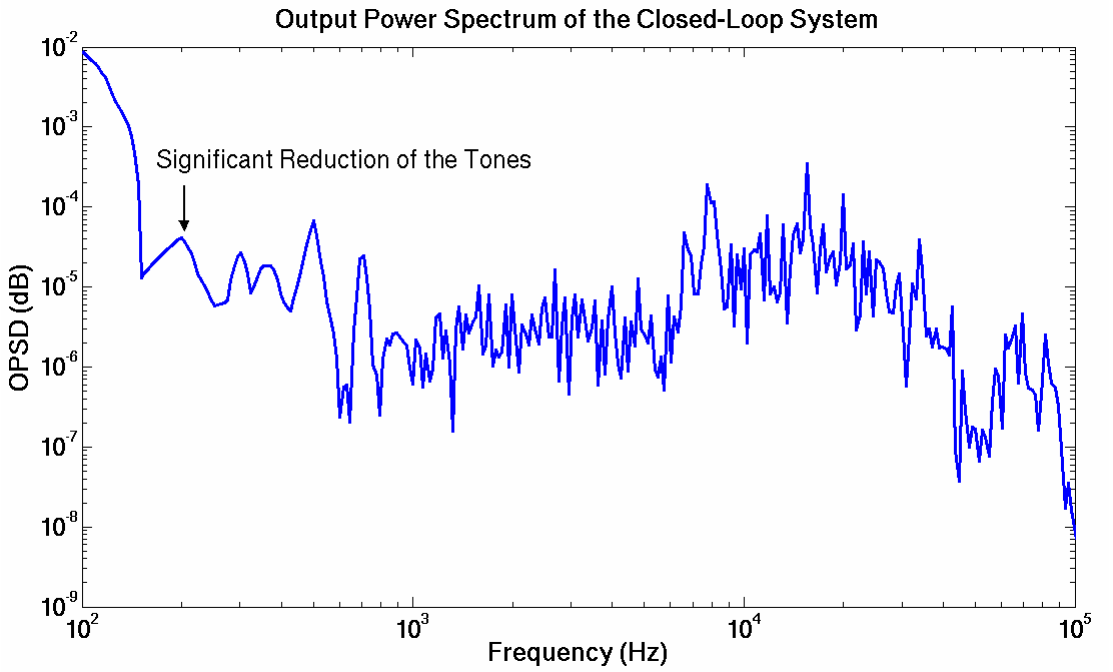

Figure 6.27: Equivalent circuit for a spring-mass-dashpot system.

In this disciplinary, the applied force *F* is analogous to the voltage, and velocity of the proof mass *u* is analogous to the current. Mass *M* is represented by an electrical inductor *L* with a value of M, the spring *K* by an electrical capacitance *C* with a value of 1/K, and the air damping *D* with an electrical resistor *R* with a value of D. Now, it is possible to add the accelerometer model to the interface circuit and do a complete simulation of the closed-loop system. Non-linearity effects of the MEMS-IC are simulated in time-domain and frequency-domain.

Figure 6.28 shows the output power spectrum of the open-loop and closed-loop configurations for a 30 milli-g input acceleration at 100 Hz. The closed-loop system was simulated with the accelerometer and actuators. The use of closed-loop system significantly reduces output tones due to the better quantization noise shaping and increased dynamic range.




(a)




(b)

Figure 6.28: Output power spectrum; (a) Open-loop system; (b) Closed-loop system.

### 6.6.2 CLOSED-LOOP PERFORMANCE MEASUREMENT

Figure 6.29 shows the microphotograph of the implemented second-order ΣΔ modulator.

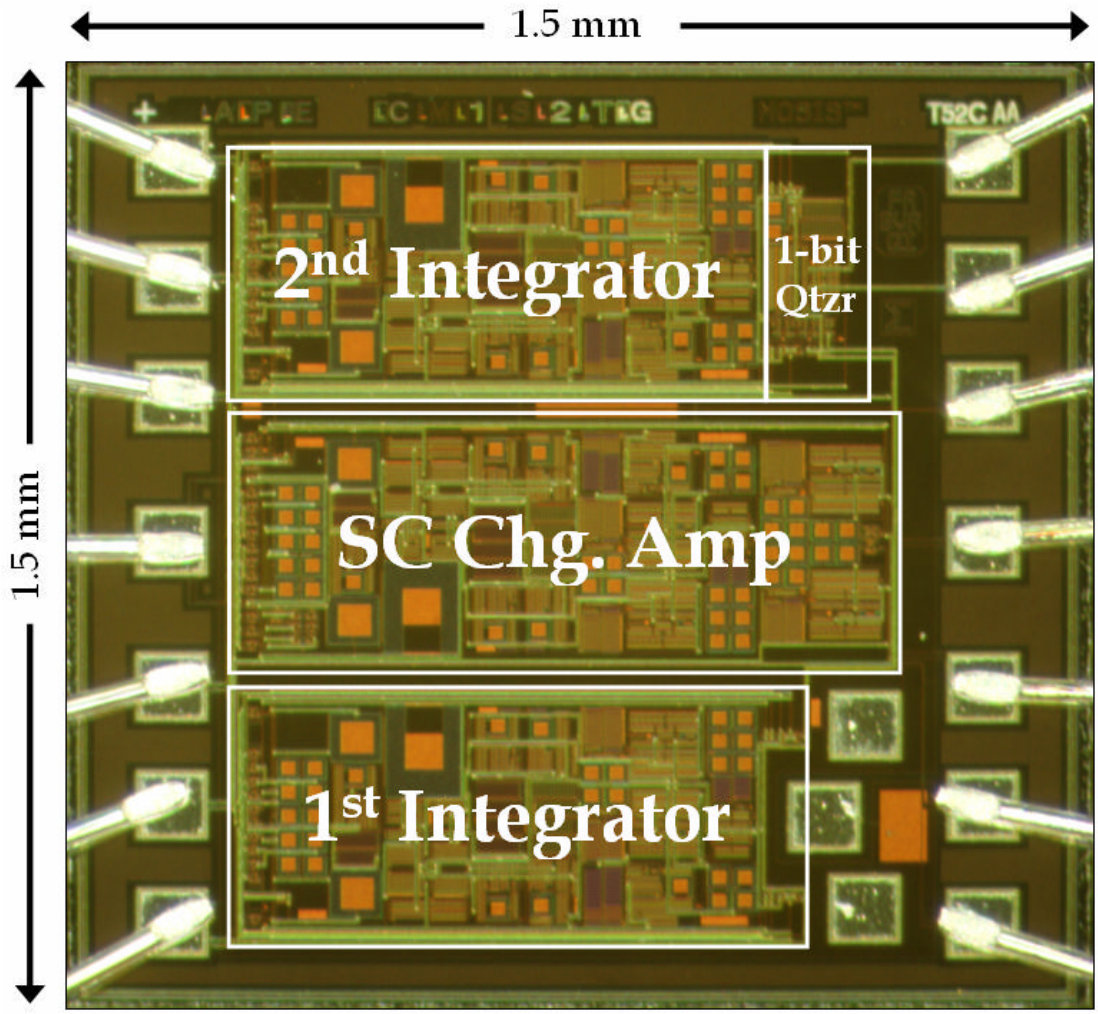



Figure 6.29: IC photomicrograph of the closed-loop ΣΔ SOI accelerometer.

On a custom-designed PCB, the accelerometer was wirebonded to the IC chip and was characterized for the sensitivity and gain (Figure 6.30).

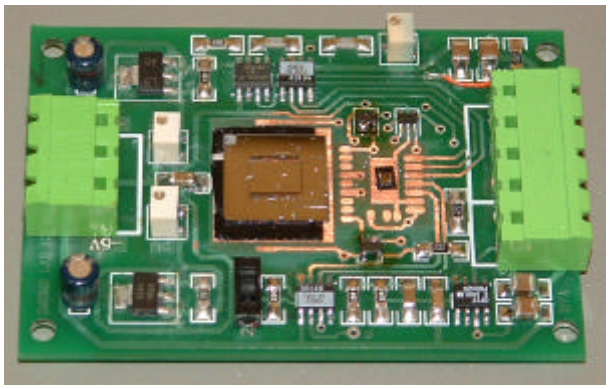


Figure 6.30: Custom-designed PCB to test the ΣΔ CMOS-SOI accelerometer.

The accelerometer has a measured sensitivity of 5 pF/g and a gain of 30 V/g. Figure 6.31 shows the time-domain response of the accelerometer to a step-input acceleration. It shows an over-damped response (non-peaking response), which is in-line with the design specification. In this test, the output of the charge amplifier (front-end block) was measured when a tilting motion was applied to the accelerometer board. As expected, the differential output swing of the IC chip is 4 V.

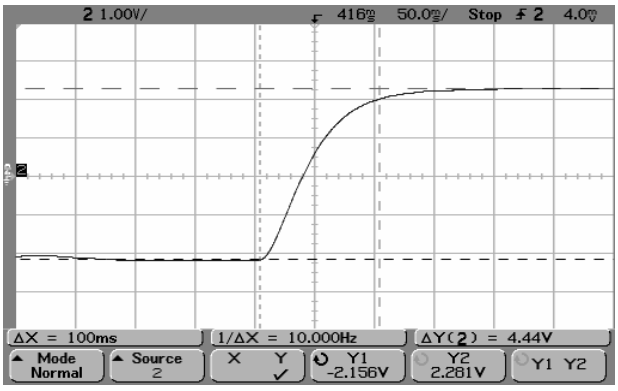



Figure 6.31: Non-peaking step response of the micro-gravity accelerometer.

Figure 6.32 shows the test set up for the open-loop and closed-loop performance measurement of the electromechanical ΣΔ CMOS-SOI accelerometer.

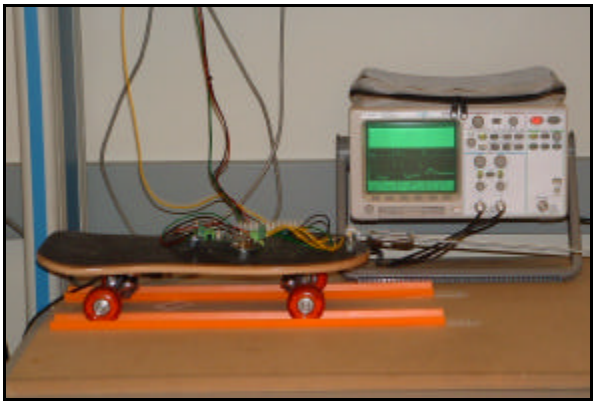


Figure 6.32: Test setup for the accelerometer test and performance measurement.

Figure 6.33 shows the open-loop and closed-loop response of the system to DC and AC (50 milli-g peak at 0.6 Hz) accelerations.

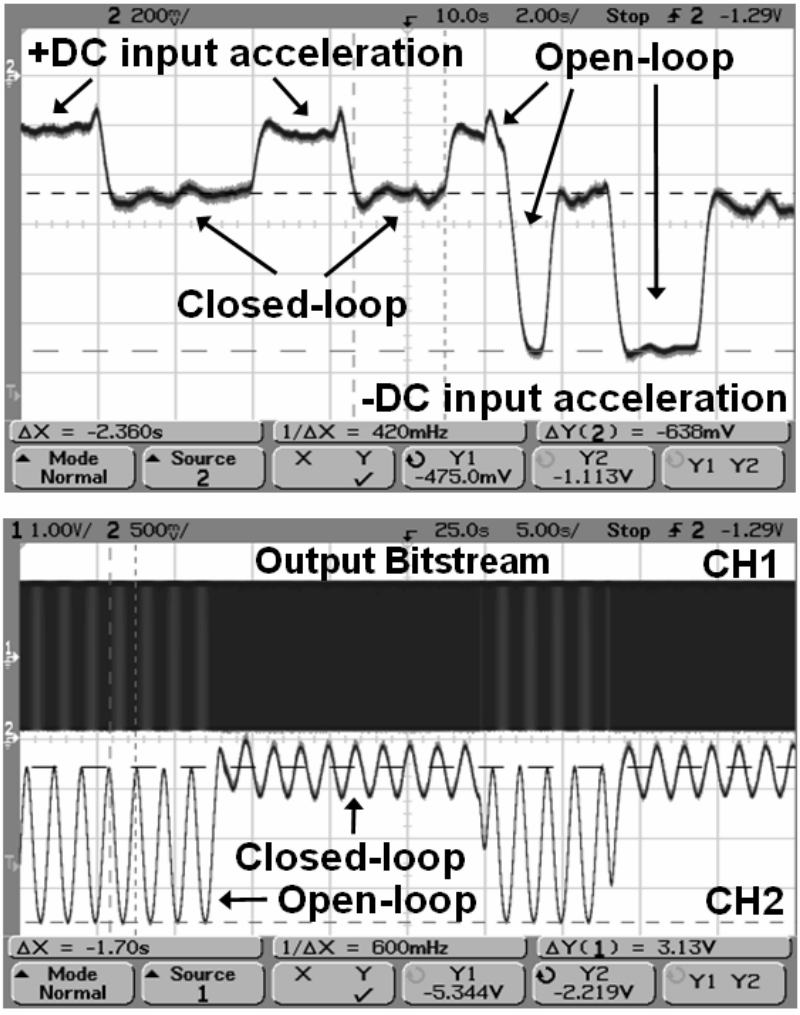



Figure 6.33: Open-loop and closed-loop responses of the ΣΔ accelerometer system.

In this figure, CH1 shows the 1-bit output Bitstream and CH2 shows the charge amplifier's output (error signal). In the open-loop system, the error signal is large, meaning the proof mass displacement is large. In the closed-loop, the output Bitstream is amplified externally and applied to the comb-drive electrodes. The electrostatic feedback force pushes the seismic mass back to the null position and the error signal reduces significantly.

Figure 6.34 shows the output noise spectrum of the interface IC, illustrating the noise shaping effect of the modulator and the up-conversion of the quantization noise. No in-band tones were observed at the output spectrum, which means the closed-loop system is functional for the input bandwidth of 500 Hz. The closed-loop system provides a noise reduction of 22 dB, corresponding to a dynamic range of 95 dB and a resolution of 15 bits (capacitive resolution of 2 aF/√Hz) at 20 Hz.

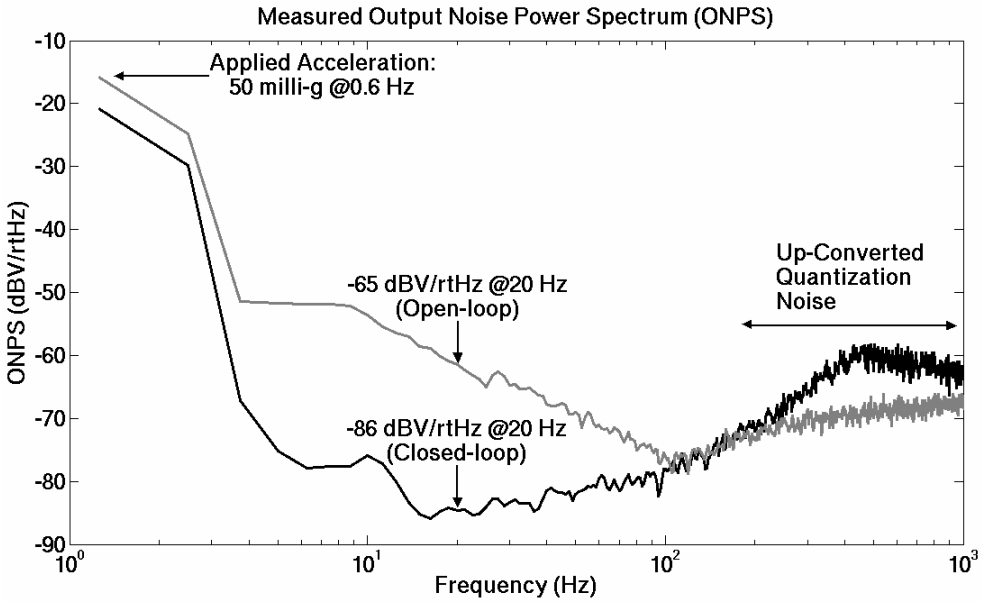



Figure 6.34: Quantization noise shaping in open-loop and closed-loop configurations.

The IC chip measures a silicon area of 2.25 $mm^2$ and consumes a low power of 4.5 mW with a sampling clock of 40 kHz. The front-end SC charge amplifier of the ΣΔ modulator was tested for the bias stability over 12 hours in a constant room

temperature. A 100000 number of samples were collected with a sampling period of 0.43 sec. The bias stability of the interface circuit was extracted using the Allan Variance analysis. Figure 6.35 shows the normalized output voltage of the circuit and the equivalent acceleration measured in 43000 sec. Figure 4.36 shows the Allan Variance plot. The IC chip measures a bias stability of 2 μg in a period of 12 hours.

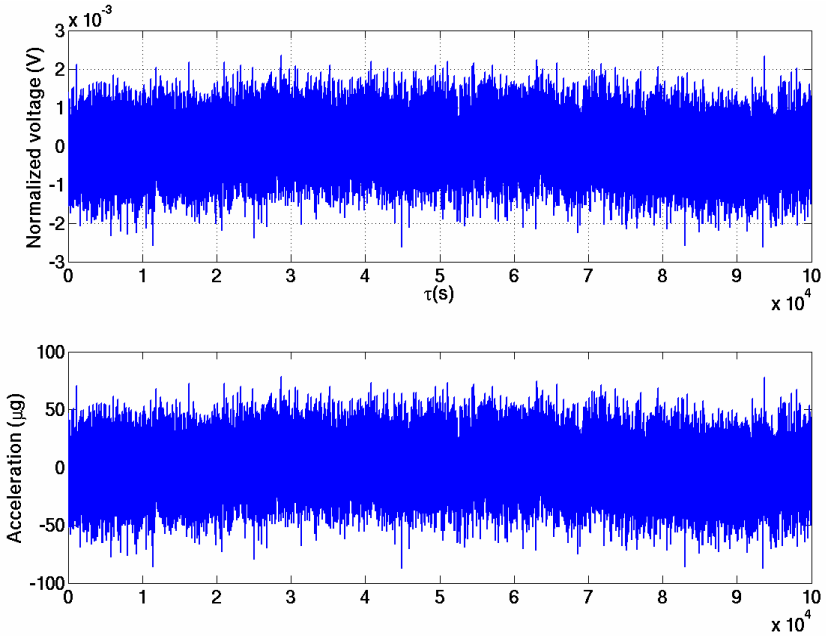



Figure 6.35: IC's normalized output voltage and equivalent acceleration.

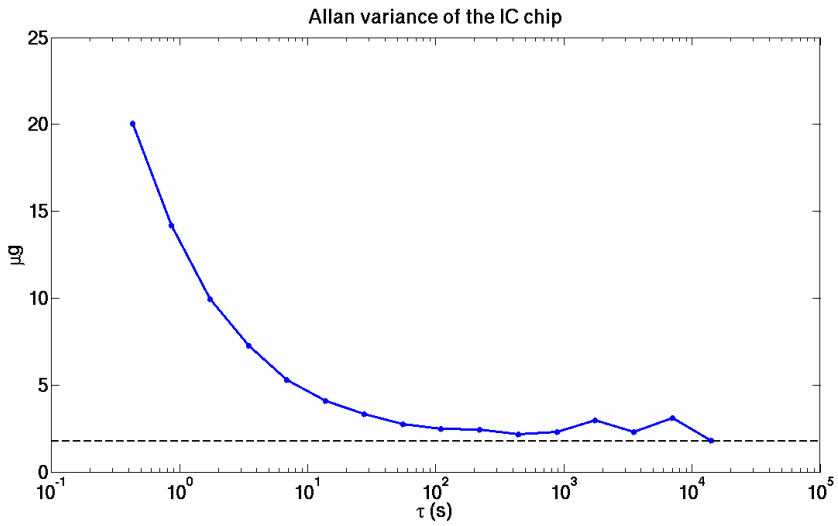



Figure 6.36: IC's Allan Variance for 100000 points of time-domain data.

Next, the IC was interfaced with the micro-gravity SOI accelerometer through the wirebonds. The accelerometer with the IC chip was tested for the bias stability in a period of 12 hours. As expected, the accelerometer was responding to the test setup vibration and external accelerations. Figure 6.37 shows the normalized output voltage and the equivalent acceleration. Figure 6.38 shows the Allan Variance plot that measures a bias stability of 10 μg for the accelerometer system.

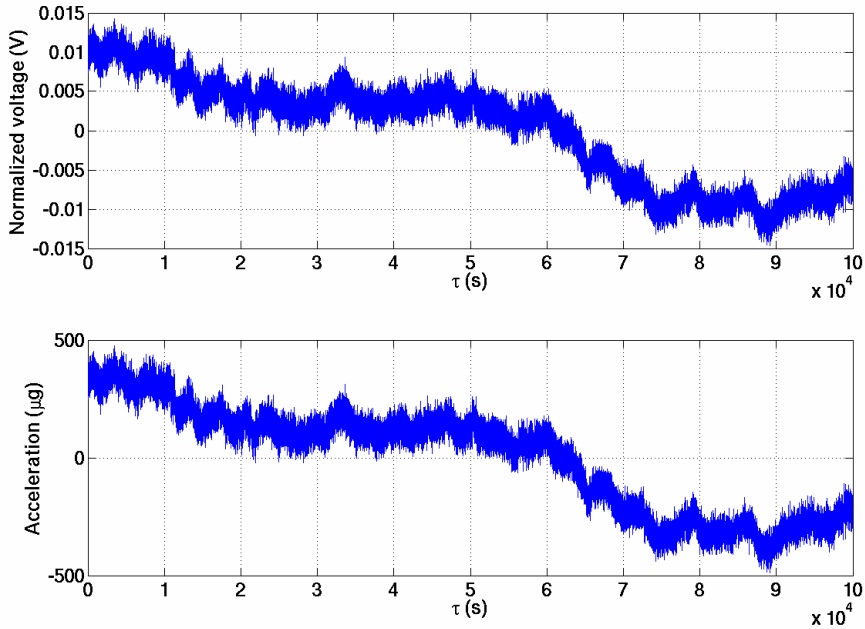



Figure6.37: Sensor' normalized output voltage and equivalent acceleration.

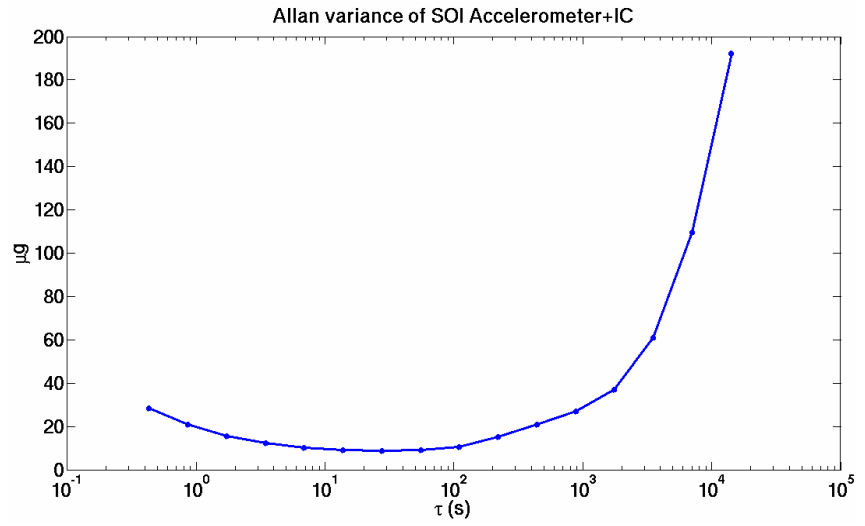



Figure 6.38: Accelerometer's Allan Variance for 100000 points of time-domain data.

Measured specifications of the closed-loop system are summarized in Table 6.2.

Table 6.2: Measured specifications of the closed-loop ΣΔ CMOS-SOI accelerometer.

| **Closed-loop Microaccelerometer-IC Performance** | |
|---|---|
| Proof mass size | 3 mm × 5 mm |
| Overall sensor size | 6 mm × 6 mm |
| Device thickness | 120 μm |
| *BNEA* | 1 μg/√Hz |
| Static sensitivity | 5 pF/g |
| Sensor bandwidth | 500 Hz |
| Front-end gain | 30 V/g |
| Front-end Max. Diff. output swing | 4 V (peak-to-peak & supply: 3 V-GND) |
| Output noise | -87 dBV/ √Hz @ 20 Hz (RBW=3 Hz) |
| *TNEA* | 4 μg/√Hz @ 20 Hz (RBW=3 Hz) |
| Capacitive resolution | 2 aF/√Hz @ 20 Hz (RBW=3 Hz) |
| Circuit's bias stability | 2 μg |
| Accelerometer's bias stability | 10 μg |
| Dynamic range | 95 dB (15 bits of resolution) |
| Sampling clock | 40 kHz |
| *OSR* | 40 |
| Power dissipation | 4.5 mW (3 V- GND) |
| Chip area | 2.25 mm2 |

## 6.7 SUMMARY

A micro-g accelerometer should maintain high performance, resolution and stability even at the presence of large background accelerations such as earth gravity. In open-loop systems, the dynamic range is limited and performance is degraded when large background accelerations exist. Therefore, closed-loop operation of the microaccelerometer is essential to improve dynamic range and linearity.

In this chapter, the implementation and characterization of a force-rebalanced high-order ΣΔ microaccelerometer with micro-gravity resolution and stability and an extended dynamic range of 95 dB was presented. The accelerometer was fabricated in low-resistivity (< 0.01 Ω.cm) 120 μm thick SOI substrates with reduced capacitive gaps using a high-yield dry-release fabrication process presented in Section 2.4. In contrast to the previously reported ΣΔ microaccelerometers, in which the mechanical transfer function of the sensor was typically the only element of the loop-filter, in this design, a second-order SC ΣΔ modulator was cascaded with the accelerometer and the front-end amplifier. High capacitive sensitivity eliminated the high gain requirement of the front-end and helped with better quantization noise shaping. The accelerometer operated in air and was designed for non-peaking response with a $BW_{-3dB}$ of 500 Hz. A 22 dB improvement in noise and hence dynamic range was achieved with a sampling clock of 40 kHz corresponding to a low oversampling ratio *(OSR)* of 40. The measured bias stability of the accelerometer was 10 μg. The interface IC consumed a current of 1.5 mA from a supply of 3 V.

# CHAPTER 7

# CONCLUSIONS AND FUTURE WORK

## 7.1 CONTRIBUTIONS

In this dissertation, the design, characterization and implementation of micro- and sub-micro-gravity capacitive solid-mass SOI accelerometers with low-power and low-noise CMOS interface ICs (open-loop and closed-loop) were investigated. The following is a list of contributions that have been achieved in this study:

1. The electromechanical design and simulation of the optimized performance capacitive SOI accelerometers was presented. Two MEMS schematic diagrams were devised to achieve micro- and sub-micro-gravity resolutions in the smallest footprint: solid proof mass with no extra mass and solid proof mass with added seismic mass. In the aspect-ratio limited SOI accelerometers, an optimized SOI thickness existed to minimize the total noise equivalent acceleration *(TNEA)* and provide micro-gravity resolution. To improve the noise performance and obtain deep micro-gravity resolution, thick silicon seismic mass on the backside of the MEMS die was kept intact. The extra seismic mass on the backside added substantial amount of mass that helped in further reduction of the mechanical and electrical noises and obtaining true micro-gravity electromechanical resolution. It should be mentioned that a similar fabrication process was developed to implement high resolution microgyroscopes in SOI substrates [91] [92].
2. A stiction-less high-yield accelerometer fabrication process was developed based on the high aspect-ratio RIE trench etching and backside dry-release. Accelerometers were released from the backside of the SOI wafers; hence no release holes were required in the proof mass. A solid proof mass with no perforation resulted in more than 25% increase in mass, smaller footprint and improved mechanical and electrical noise performances. Through innovation in the fabrication process, the resolution and sensitivity of the dry-released SOI accelerometers were each improved by 10× to achieve, for the first time,

deep sub-micro-gravity resolution in a small footprint (<0.5cm$^2$). The improved fabrication process enabled increase of the seismic mass (to suppress the mechanical noise) and reduction of gap sizes (to increase the sensitivity and suppress the electrical noise), independently. In the other words, the device sensitivity was improved by reduction of the capacitive gap size through the deposition of a layer of doped LPCVD poly silicon. In addition, the device mechanical noise floor was improved by increasing the solid seismic mass through saving some part of the handle layer attached to the proof mass. More than five devices were tested for the functionality and performance. All of them demonstrated true sub-micro-gravity resolution.

3. A generic capacitive interface architecture based on a programmable front-end charge amplifier and back-end first-order ΣΔ modulator was introduced and implemented in a 2.5 V 0.25μm CMOS technology. The ΣΔ modulator is effectively decoupled from the sensor to achieve optimized performance regardless of the size of the sensor capacitance. In addition, the front-end can be sampled at low frequency (especially useful when the sensor capacitance and hence the time constants are large), while the back-end is clocked at a higher frequency to up-convert the quantization noise more efficiently.

4. The efficiency of the CDS scheme in low-frequency noise cancellation was quantified with simulation and was verified by comparing implementations with and without CDS.

5. A new reference-capacitor-less front-end IC was designed and implemented that has the ability of interfacing capacitive sensors with large rest capacitors including bulk-micromachined accelerometers. It eliminated area consuming on-chip reference capacitors and increased the versatility of the front-end block. In this architecture, the proof mass was tied to a constant voltage source ($0.5V_{DD}$) at all times and was never switched. This in turn simplified the digital clock generator circuit and reduced the charge injection noise. The front-end block was used in two different open-loop architectures. One was a band-limited analog output circuit to interface with sub-micro-gravity SOI accelerometers. The other one was a digital output circuit (ΣΔ modulator) wirebonded to micro-gravity accelerometers. A 2.5 V 0.25 μm and a 3 V 0.5

μm N-well CMOS were used to fabricate the interface ICs. A complete characterization of the noise and power performances was provided for each of the MEMS-IC implementations. The accelerometer system was characterized for the static and dynamic responses.

6. In the last part of the dissertation, the design, implementation and characterization of a new monolithic electromechanical high-order ΣΔ microaccelerometer with micro-gravity resolution and stability and an extended dynamic range of 95 dB was presented. The overall order of the closed-loop (force-rebalanced) system was 4, suppressing the in-band quantization noise by more than 20 dB. The interface circuit is implemented in a standard 3 V 0.5 μm N-well CMOS process and consumes a low-power of 4.5 mW. The IC chip provides a 1-bit PWM output that is amplified and fed back to the accelerometer through a set of comb-drive actuators. The main advantage of using comb-drive actuator (compared to parallel-plate actuator) is that the electrostatic feedback force does not depend on the proof mass position, which provides linearity and simplifies the design. Since the comb-drive actuator is implemented in thick SOI with reduced gap, the feedback force will be strong enough to null the movement of the large proof mass. . The output noise of the closed-loop system is measured to be -87 dBV/√Hz at 20 Hz with a resolution bandwidth (RBW) of 3 Hz. The system without electromechanical feedback measures a noise floor of -65 dBV/√Hz at 20 Hz, which is dominated with the in-band quantization noise. A 22 dB improvement in quantization noise and hence dynamic range was achieved through the closed-loop operation with a sampling clock of 40 kHz corresponding to an oversampling ratio *(OSR)* of 40.

A comparison between the presented open-loop sub-micro-gravity capacitive CMOS-SOI accelerometer and two other state-of-the-art accelerometers from Applied MEMS, Inc [96] and Freescale Semiconductor, Inc [97] is provided in Table 7.1. To the best of the author's knowledge, this SOI accelerometer is one of the most sensitive capacitive MEMS accelerometers that have been reported so far.

Table 7.1: A comparison between our designed accelerometer and two other accelerometers from Applied MEMS, Inc and Freescale Semiconductor, Inc.

| Parameter | Si-Flex™ SF1500L [96] | MMA6270Q [97] | Sub-micro-g SOI |
|---|---|---|---|
| Full-scale | ±3g | ±1.5g Dual | ±30 milli-g |
| *TNEA* | 500 ng/√Hz (1) | 350 μg/√Hz | 213 ng/√Hz |
| Sensitivity | 1.2 V/g | 0.8 V/g | 105 V/g |
| *DR* | 120 dB | NA | 103 dB |
| Bandwidth | DC-1.5kHz | DC-350 Hz | DC-200 Hz |
| Supply | ±6 V to ±15 V | 3.3 V (1) | 3 V |
| Output format | Analog | Analog | Analog |
| Dissipation | NA | 1.65 mW | 4 mW |

(1) Typical value

## 7.2 FUTURE DIRECTION

The capacitive SOI accelerometers described in this dissertation were single axis, wirebonded to the IC chip (two-chip solution) with no wafer-level packaging. Packaging of the accelerometers is an important research area that needs more exploration. Although, we have used open-cavity MEMS-IC packaging, there are other MEMS solutions to do monolithic 3-Axis MEMS-IC packaging in a wafer-level, which is an important feature for commercialization of the accelerometers [93].

In many applications, it is important to measure the acceleration in three-spatial dimensions. The other potential research can be concentrated on the design and implementation of biaxial or triaxial micro-gravity SOI accelerometers in a single SOI

embodiment with a small form-factor that are wirebonded to a single interface circuit. A functional block diagram of such a design is shown in Figure 7.1.

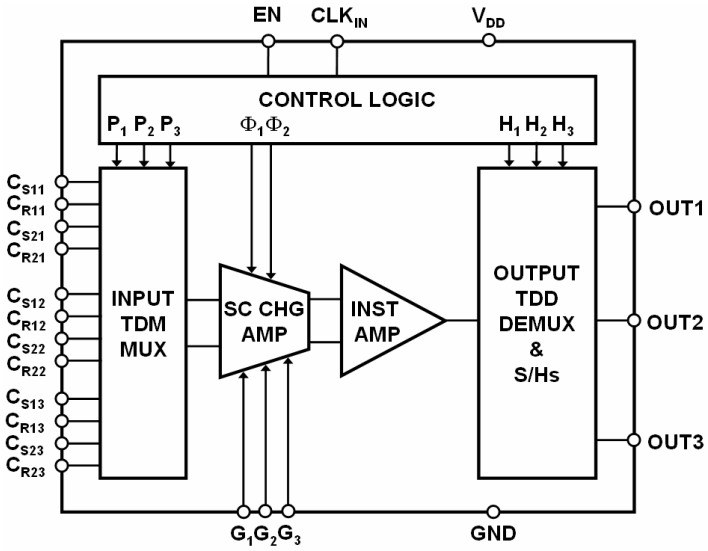



Figure 7.1: Functional block diagram of a triaxial multiplexed accelerometer.

In this figure, the input ports of $C_{S11}$, $C_{R11}$, $C_{S21}$, $C_{R21}$, $C_{S12}$, $C_{R12}$, $C_{S22}$, $C_{R22}$, $C_{S13}$, $C_{R13}$, $C_{S23}$, and $C_{R23}$ denote changing capacitances of 3 different fully-differential capacitive MEMS accelerometers. *EN* is the chip enable input. Each accelerometer is selected through a time-division multiplexer (TDM) and connected to the only switched-capacitor charge amplifier (SC CHG AMP) in the front-end. The amplifier has a fully differential scheme, to suppress the common-mode noises, with a binary-weighted programmable gain. Differential-to-single-ended conversion is utilized by an instrumentation amplifier. The output signal of each accelerometer is eventually separated by a time-division-demultiplexer (TDD). Each output channel passes through a buffered sample-and-hold (S&H) and *RC* low-pass filter. Figure 7.2 demonstrates the circuit schematic of the interface IC. The control logic block should provide the necessary sequential clocks of $P_1$, $P_2$, $P_3$, $H_1$, $H_2$, and $H_3$ along with the SC sampling clocks.

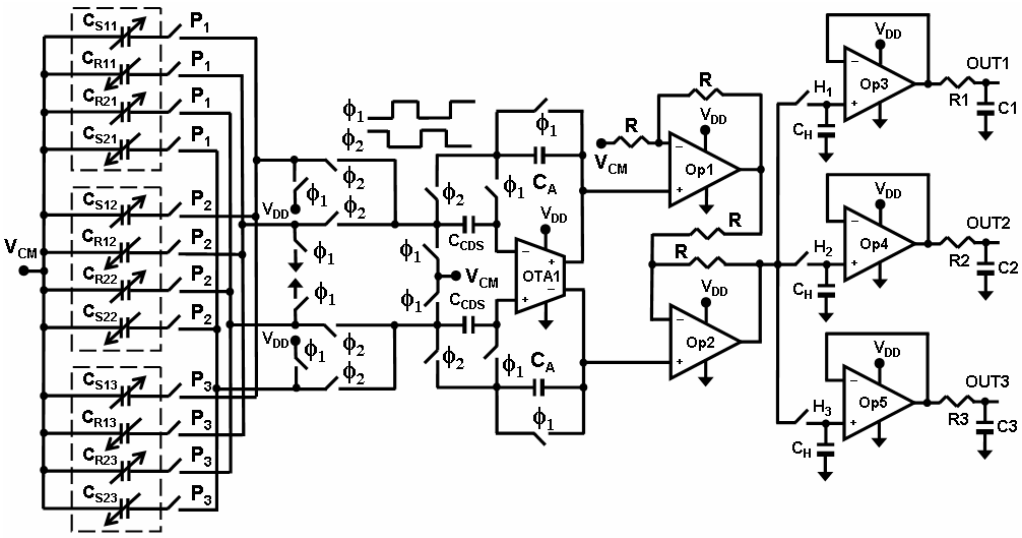



Figure 7.2: Schematic diagram of a multi-channel-accelerometer readout IC.

Figure 7.3 shows the sequence of the clocks required in SC amplifier, TDM and TDD blocks.

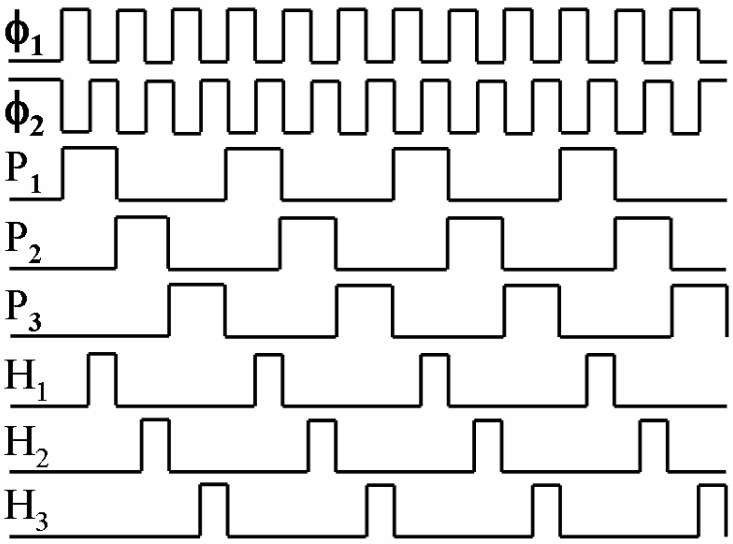



Figure 7.3: SC, TDM and TDD timing clocks.

This architecture should demonstrate the stat-of-the-art 3-axis SOI accelerometer-IC with smallest footprint and lowest power dissipation that is competitive with other commercially available micro-gravity accelerometers [94].

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